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(54) **SYSTEM AND METHODS FOR EXTRACTION OF THRESHOLD AND MOBILITY PARAMETERS IN AMOLED DISPLAYS**

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(58) **Field of Classification Search**
None
See application file for complete search history.

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(57) **ABSTRACT**

A system to improve the extraction of transistor and OLED parameters in an AMOLED display includes a pixel circuit having an organic light emitting device, a drive device to provide a programmable drive current to the light emitting device, a programming input to provide the programming signal, and a storage device to store the programming signal. A charge-pump amplifier has a current input and a voltage output. The charge-pump amplifier includes an operational amplifier in negative feedback configuration. The feedback is provided by a capacitor connected between the output and the inverting input of the operational amplifier. A common-mode voltage source drives the non-inverting input of the operational amplifier. An electronic switch is coupled across the capacitor to reset the capacitor. A switch module including the input is coupled to the output of the pixel circuit and an output is coupled to the input of the charge-pump amplifier.

16 Claims, 12 Drawing Sheets

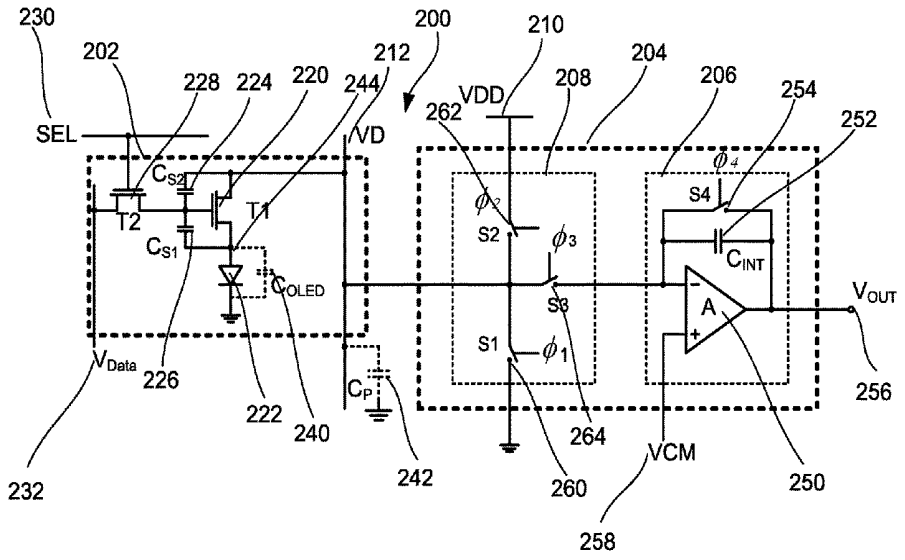

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FIG. 1

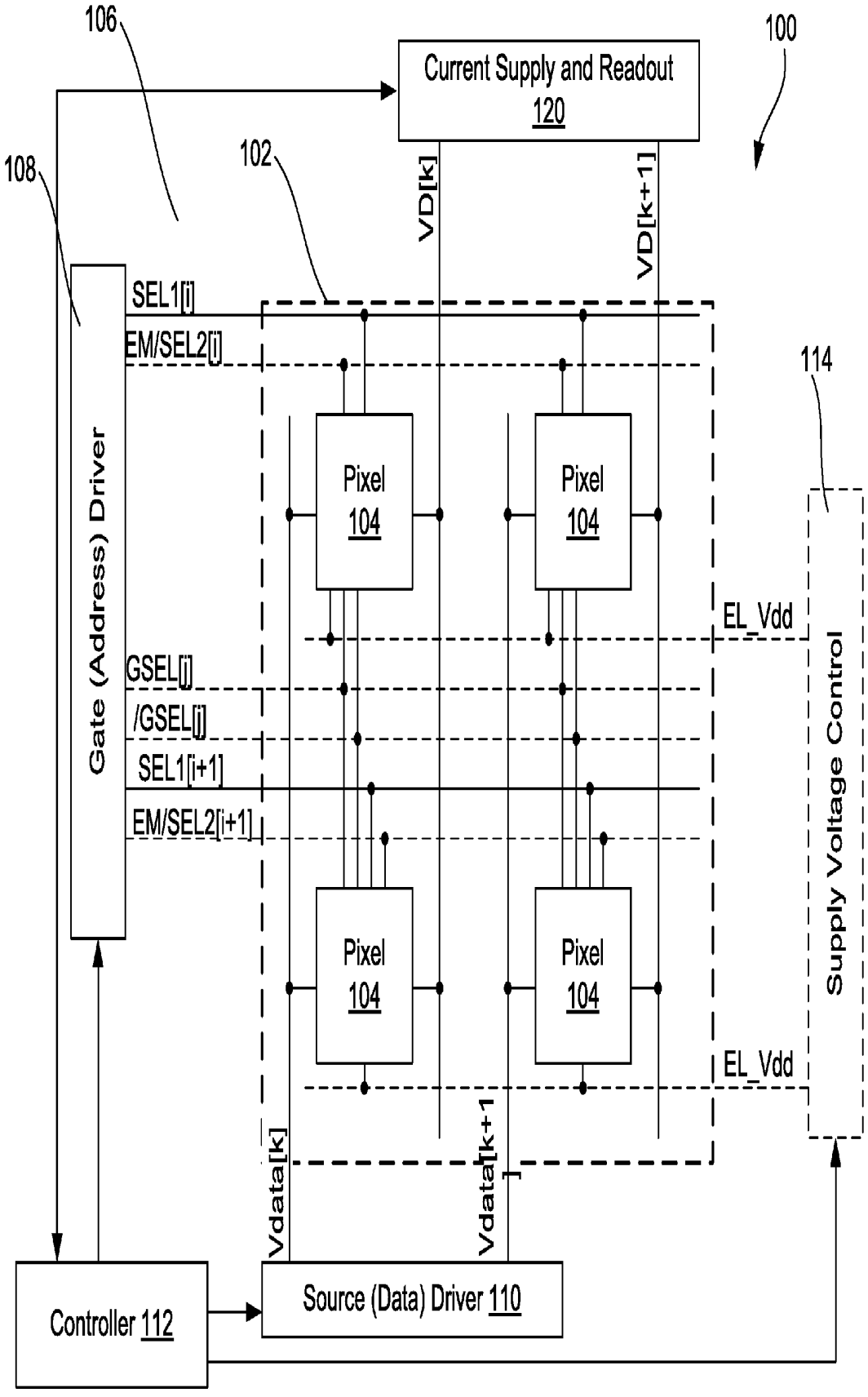

106
100
Current Supply and Readout
120
108
102
VD[k]
VD[k+1]
SEL1[i]
EM/SEL2[i]
114
Gate (Address) Driver
Pixel
104
Pixel
104
EL_Vdd
GSEL[j]
/GSEL[j]
SEL1[i+1]
EM/SEL2[i+1]
Supply Voltage Control
Pixel
104
Pixel
104
EL_Vdd
Vdata[k]
Vdata[k+1]
Controller 112
Source (Data) Driver 110

FIG. 2

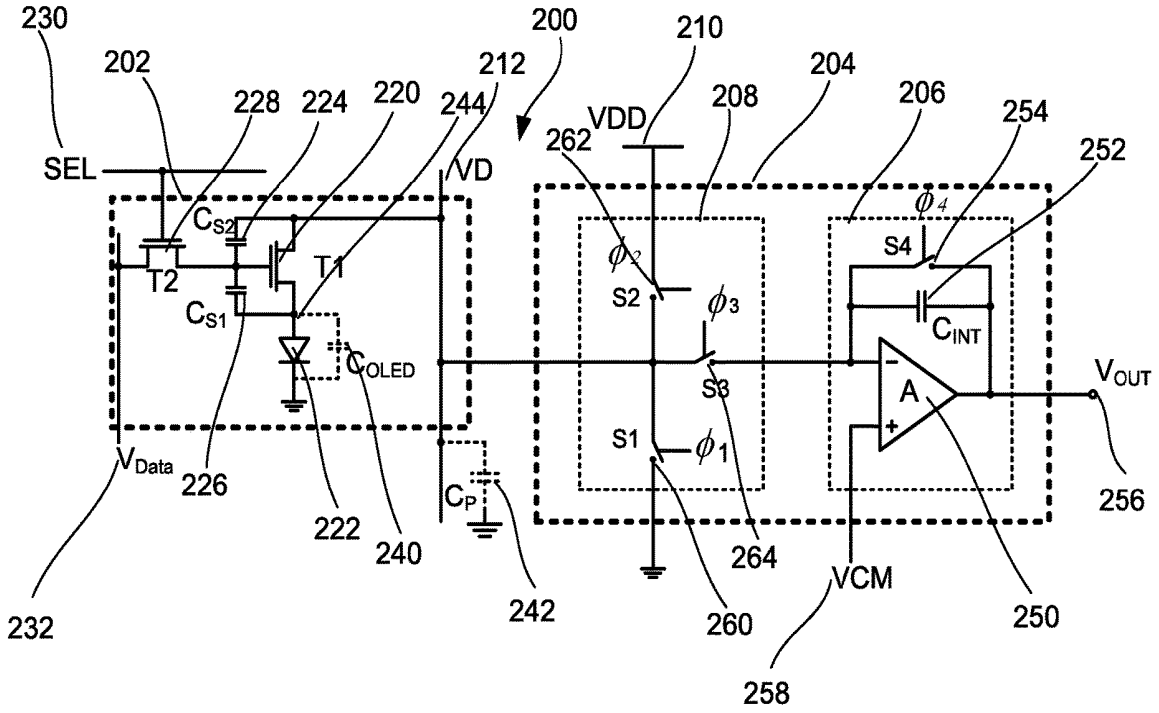

230
202
228
224
220
244
212
200
210
204
206
254
252
SEL
VD
VDD
262
208
ϕ_4
S4
C_{S2}
ϕ_2
T2
T1
S2
ϕ_3
C_{INT}
C_{S1}
C_{OLED}
S3
A
V_{OUT}
S1
ϕ_1
V_{Data}
226
222
240
C_P
242
264
256
VCM
260
250
232
258

FIG. 3A

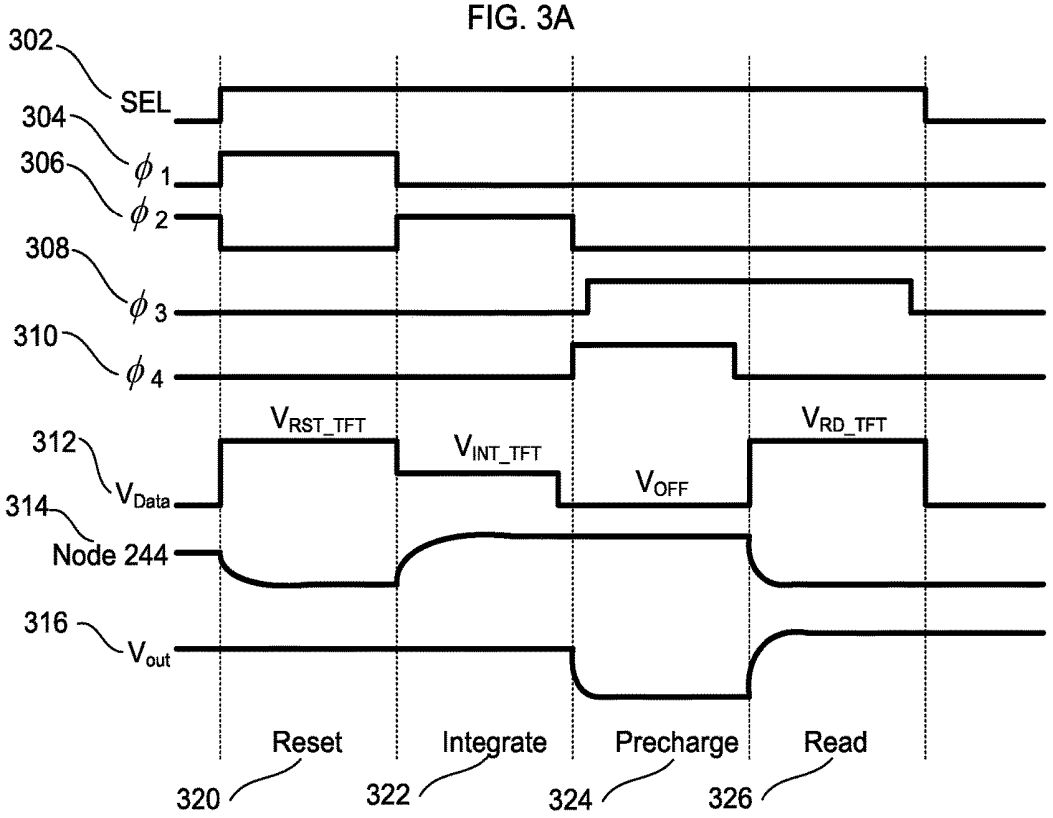

302
SEL
304
ϕ_1
306
ϕ_2
308
ϕ_3
310
ϕ_4
312
V_{Data}
V_{RST_TFT}
V_{INT_TFT}
V_{OFF}
V_{RD_TFT}
314
Node 244
316
V_{out}
Reset
Integrate
Precharge
Read
320
322
324
326

FIG. 3B

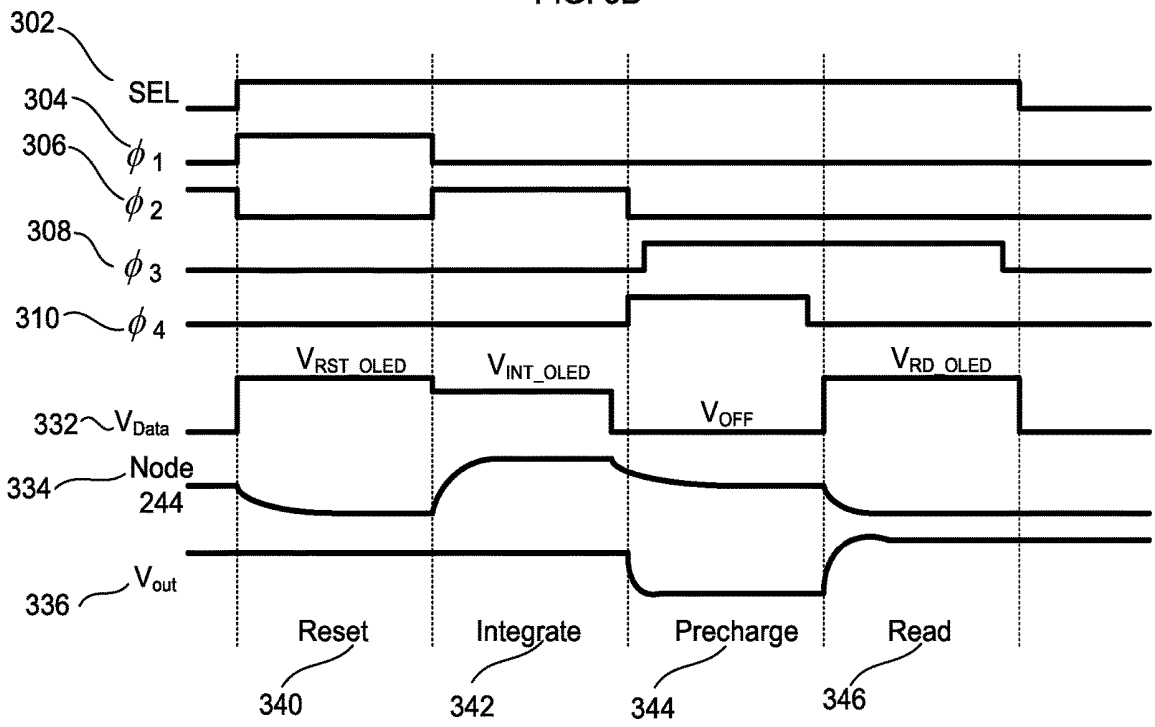

302
SEL
304
ϕ_1
306
ϕ_2
308
ϕ_3
310
ϕ_4
332
V_{Data}
V_{RST_OLED}
V_{INT_OLED}
V_{OFF}
V_{RD_OLED}
334
Node 244
336
V_{out}
Reset
Integrate
Precharge
Read
340
342
344
346

FIG. 3C

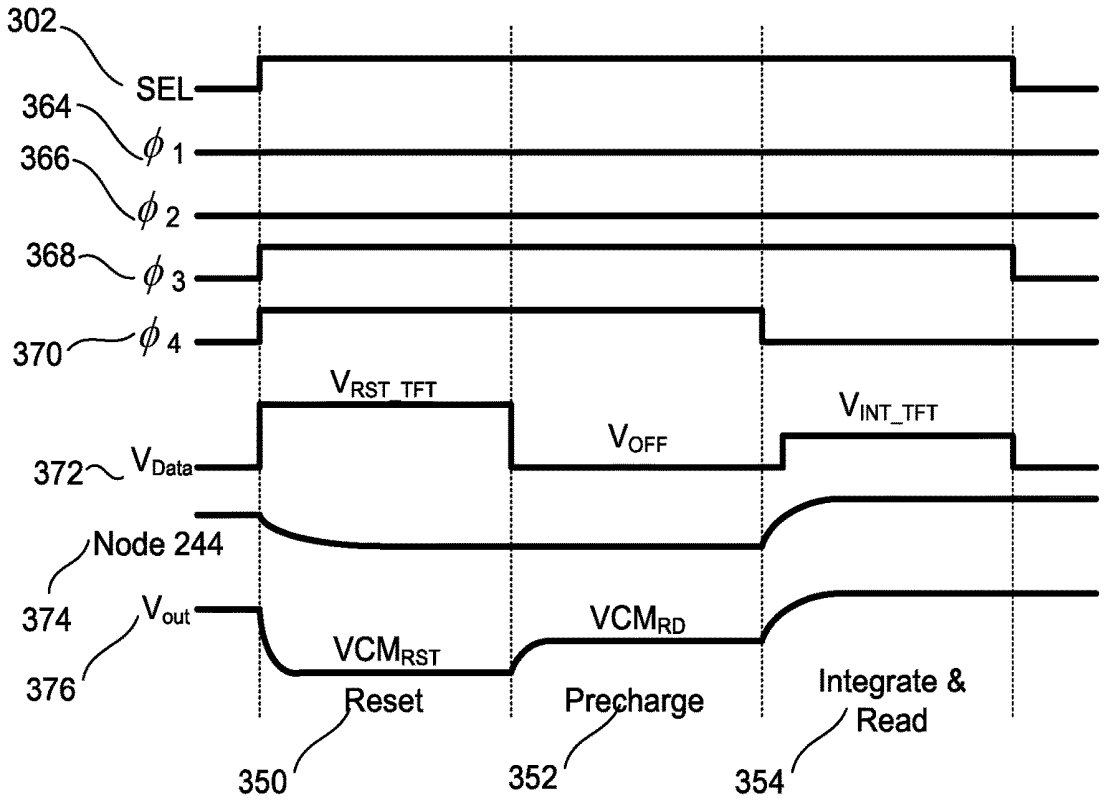

302
SEL
364
ϕ 1
366
ϕ 2
368
ϕ 3
370
ϕ 4
V_{RST_TFT}
V_{OFF}
V_{INT_TFT}
372
V_{Data}
Node 244
374
V_{out}
376
VCM_{RST}
VCM_{RD}
Reset
Precharge
Integrate & Read
350
352
354

FIG. 4A

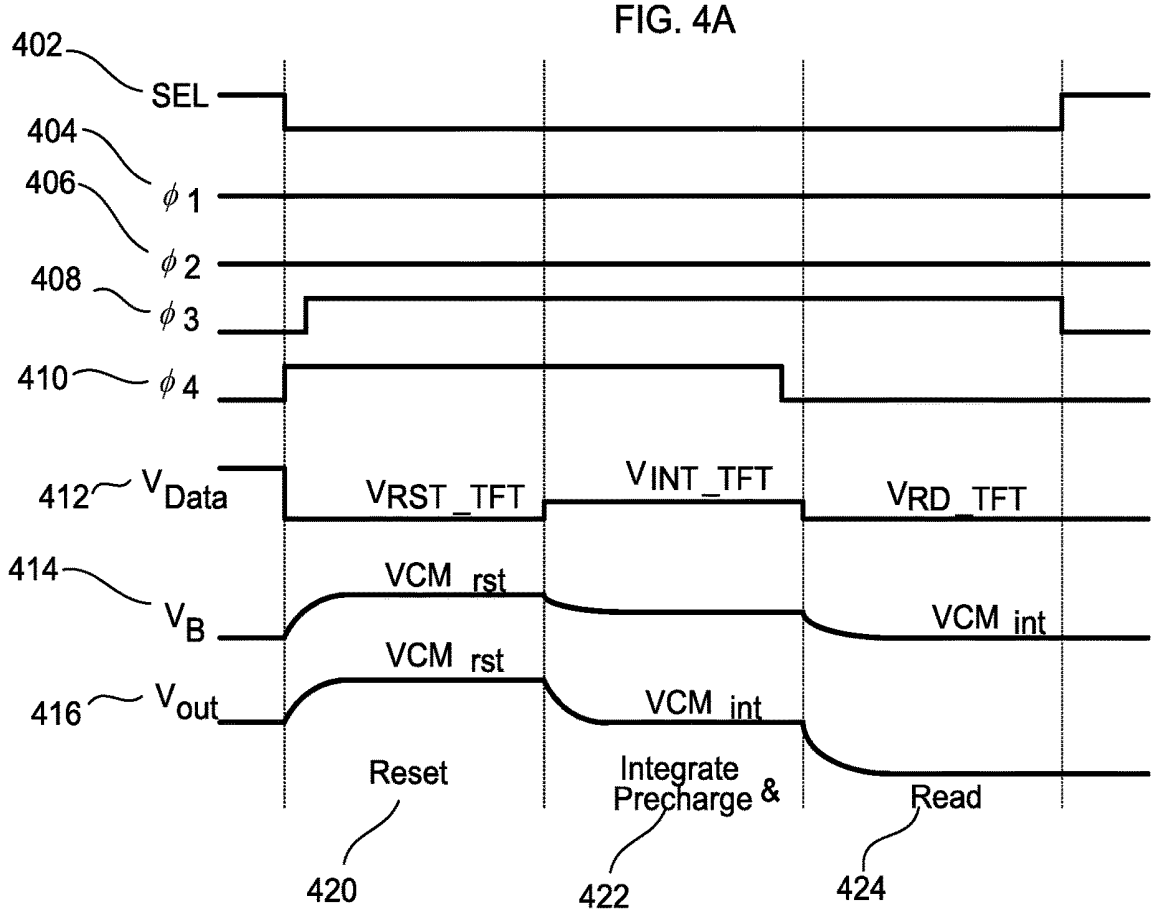

402
SEL
404
ϕ 1
406
ϕ 2
408
ϕ 3
410
ϕ 4
412
V_{Data}
V_{RST_TFT}
V_{INT_TFT}
V_{RD_TFT}
414
V_B
VCM rst
VCM int
416
V_{out}
VCM rst
VCM int
Reset
Integrate & Precharge
Read
420
422
424

FIG. 4B

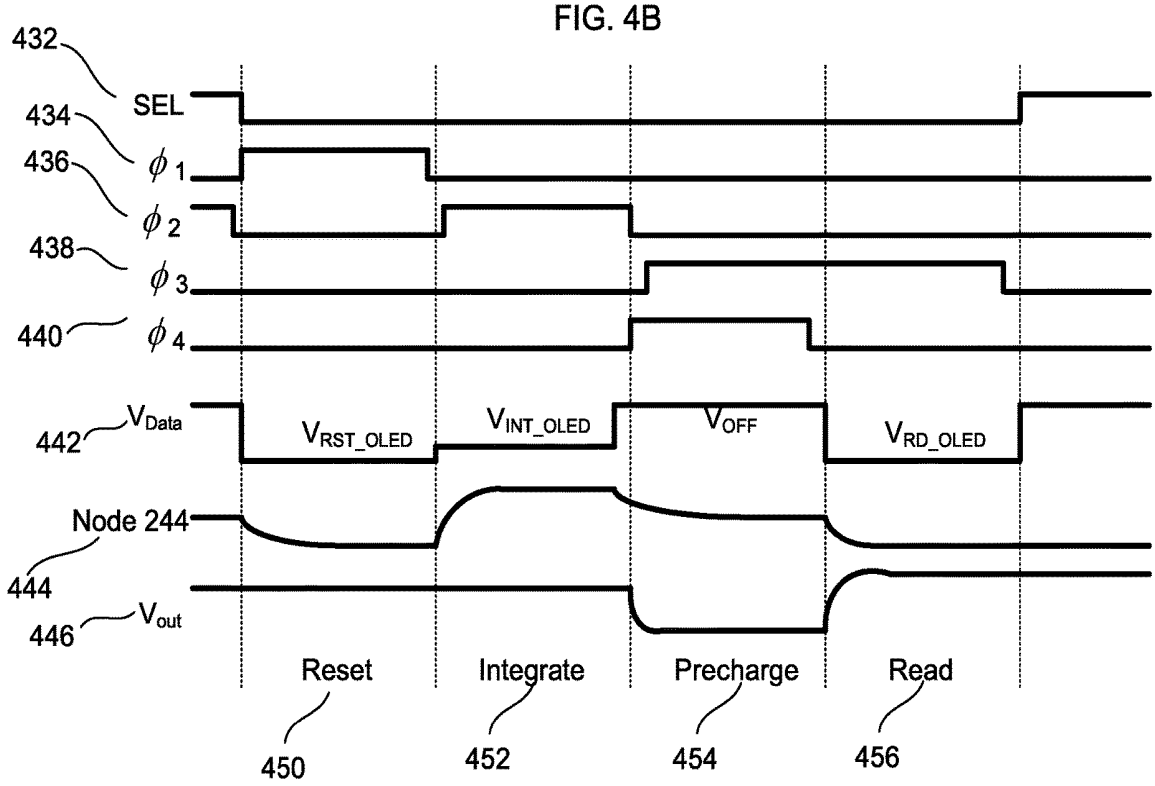

432
SEL
434
ϕ_1
436
ϕ_2
438
ϕ_3
440
ϕ_4
442
V_{Data}
V_{RST_OLED}
V_{INT_OLED}
V_{OFF}
V_{RD_OLED}
Node 244
444
446
V_{out}
Reset
Integrate
Precharge
Read
450
452
454
456

FIG. 4C

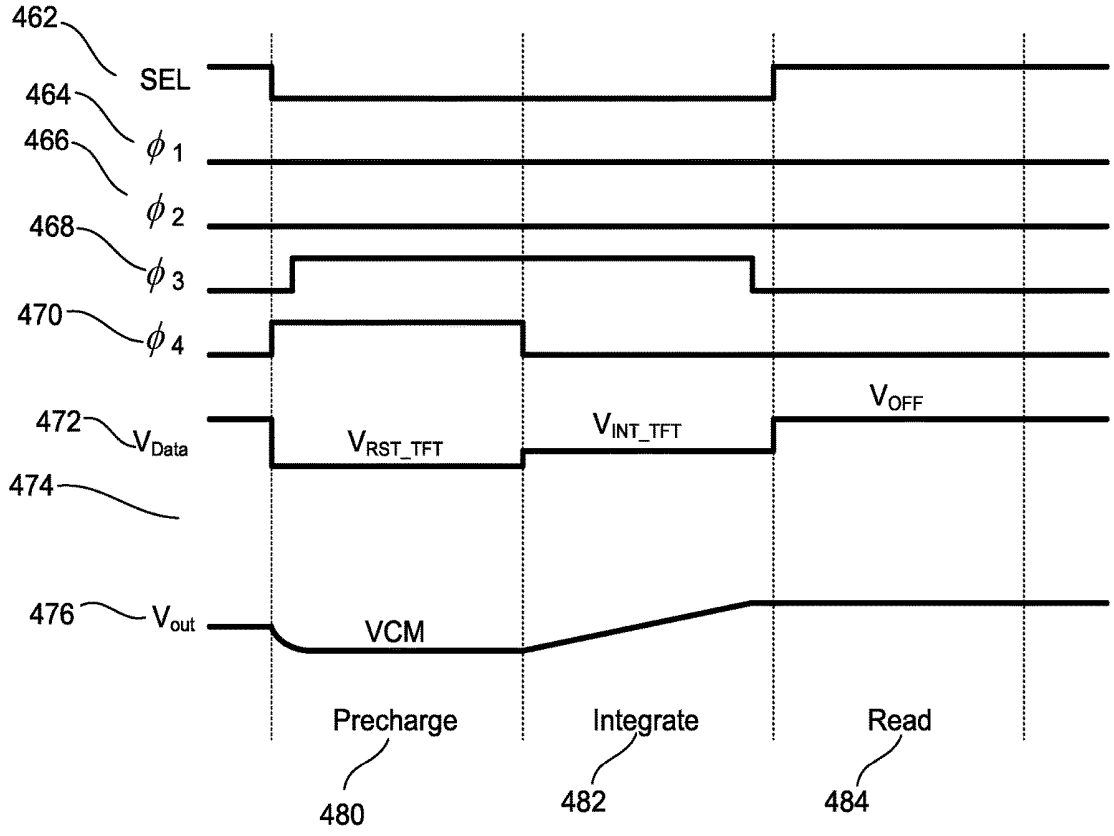

462
SEL
464
ϕ_1
466
ϕ_2
468
ϕ_3
470
ϕ_4
472
V_{Data}
V_{RST_TFT}
V_{INT_TFT}
V_{OFF}
474
476
V_{out}
VCM
Precharge
Integrate
Read
480
482
484

FIG. 4D

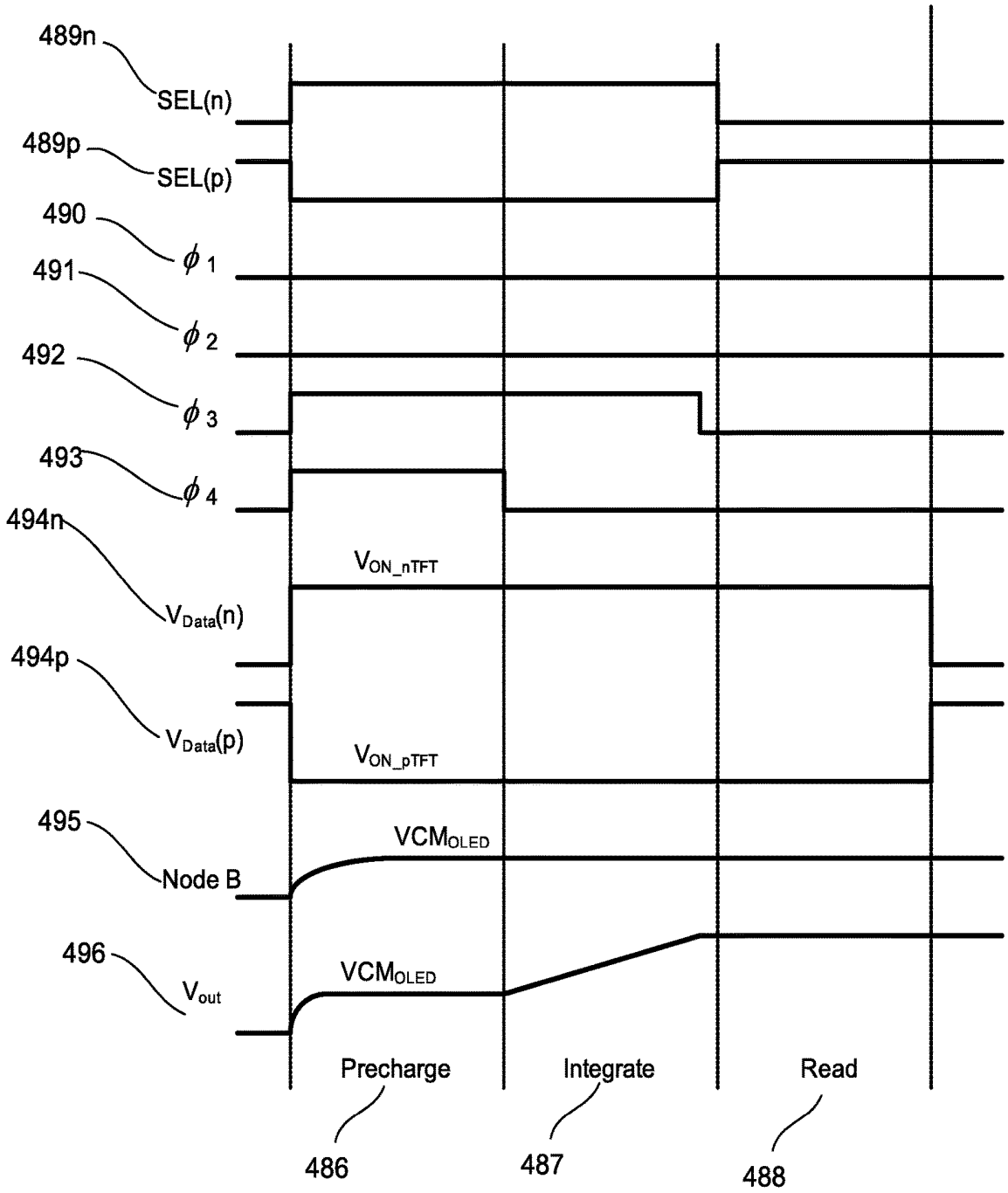

489n
SEL(n)
489p
SEL(p)
490
ϕ_1
491
ϕ_2
492
ϕ_3
493
ϕ_4
494n
V_{ON_nTFT}
$V_{Data}(n)$
494p
$V_{Data}(p)$
V_{ON_pTFT}
495
VCM_{OLED}
Node B
496
VCM_{OLED}
V_{out}
Precharge
Integrate
Read
486
487
488

FIG. 5

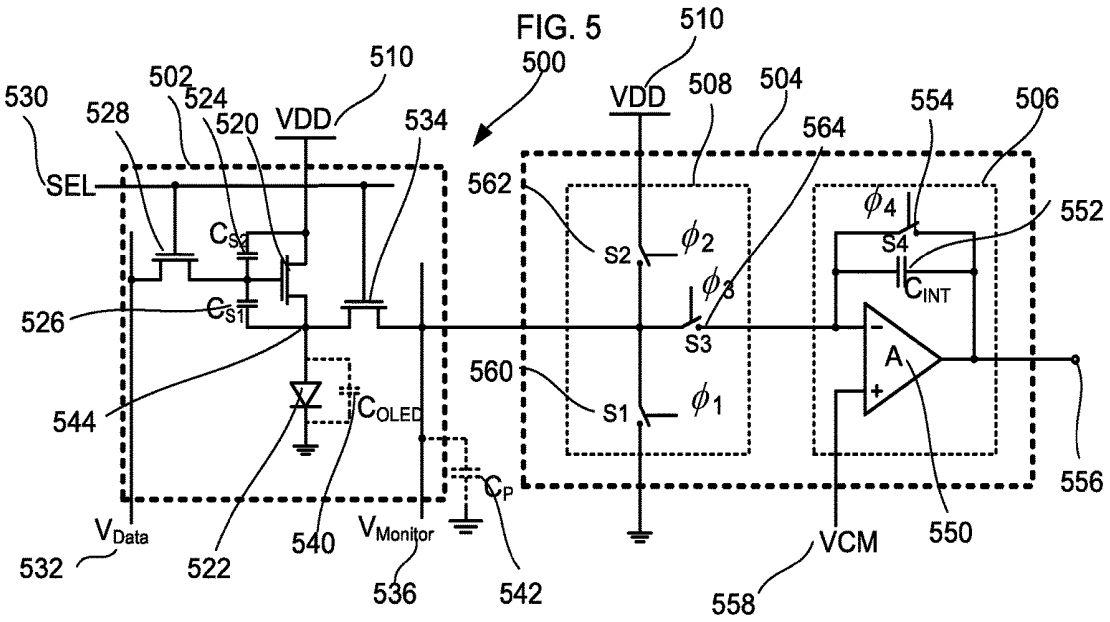

500
510
VDD
508
504
554
506
530
528
502
524
520
534
562
564
552
SEL
C_{S2}
C_{S1}
526
544
C_{OLED}
C_P
S2
ϕ_2
ϕ_3
S3
S1
ϕ_1
ϕ_4
S4
C_{INT}
A
560
556
550
VCM
558
V_{Data}
532
522
540
$V_{Monitor}$
536
542

FIG. 6A

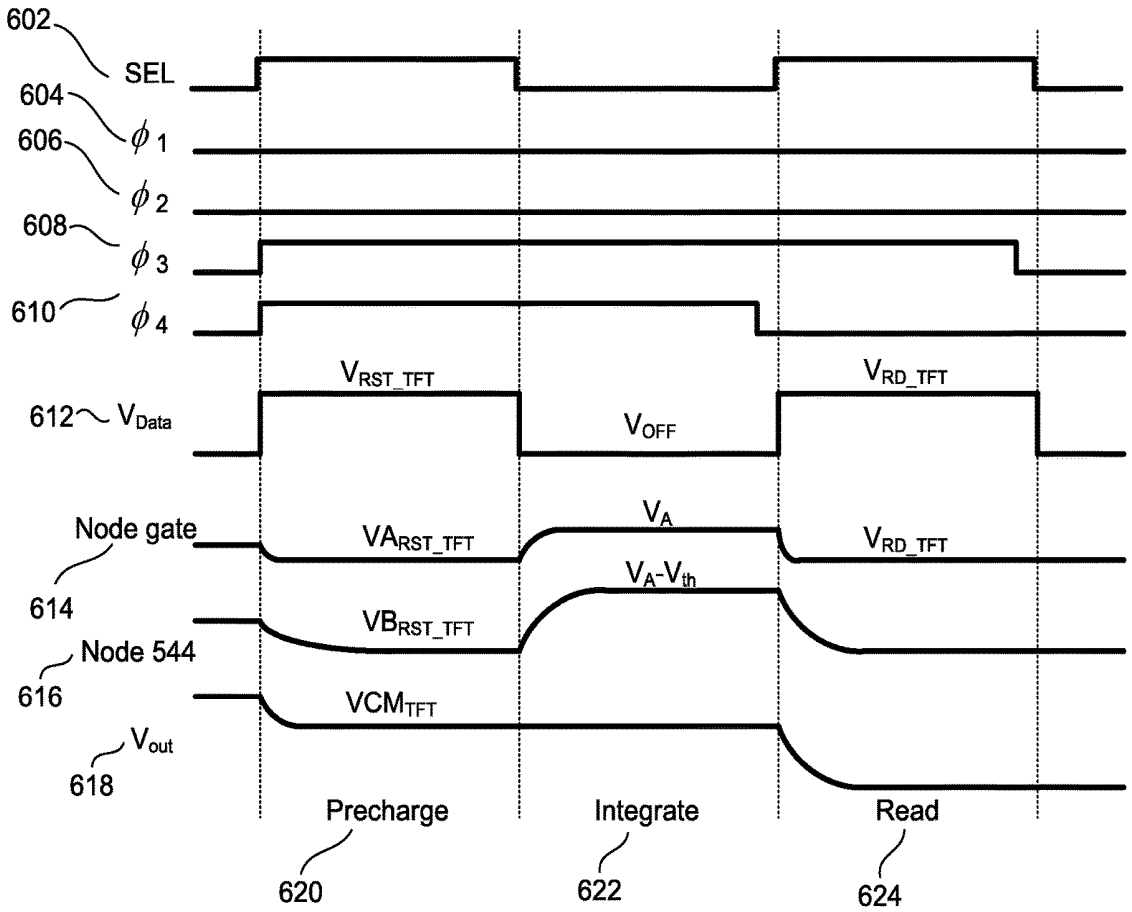

602
SEL
604
ϕ_1
606
ϕ_2
608
ϕ_3
610
ϕ_4
612
V_{Data}
V_{RST_TFT}
V_{OFF}
V_{RD_TFT}
Node gate
614
VA_{RST_TFT}
V_A
V_{RD_TFT}
VB_{RST_TFT}
V_A-V_{th}
Node 544
616
VCM_{TFT}
V_{out}
618
Precharge
620
Integrate
622
Read
624

FIG. 6B

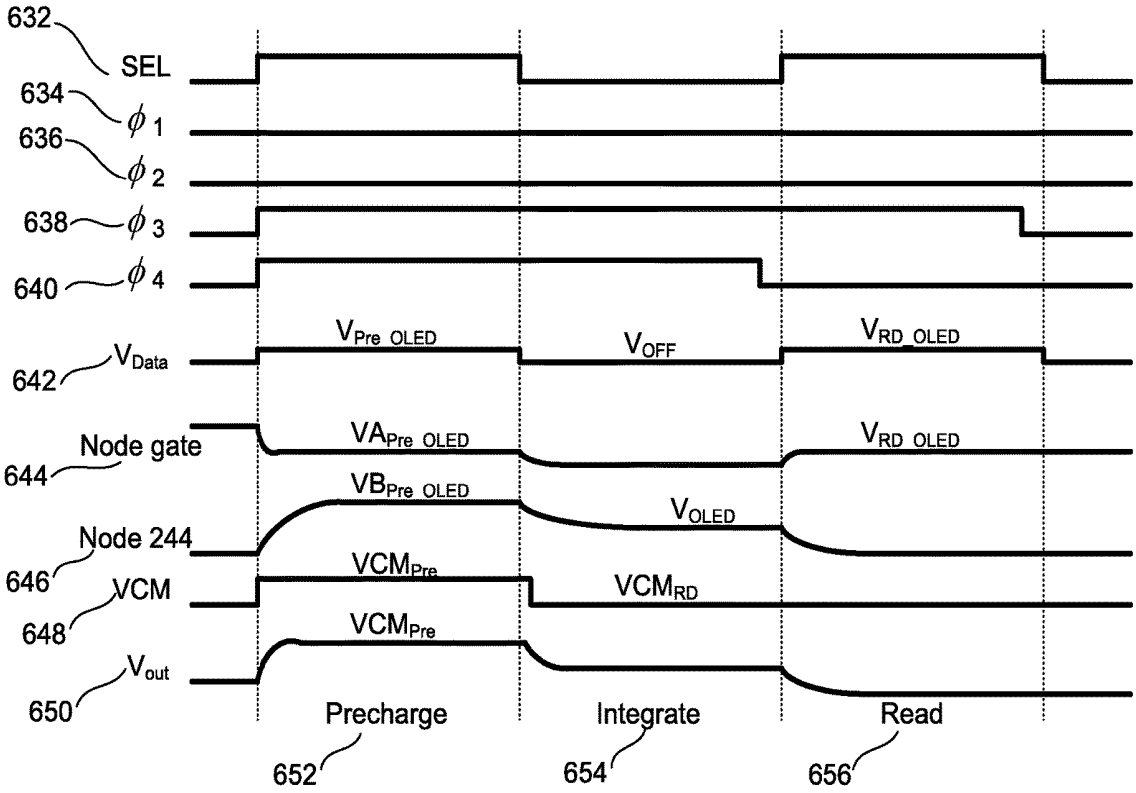

632
SEL
634
ϕ_1
636
ϕ_2
638
ϕ_3
640
ϕ_4
642
V_{Data}
$V_{Pre\ OLED}$
V_{OFF}
V_{RD_OLED}
Node gate
644
$VA_{Pre\ OLED}$
$V_{RD\ OLED}$
$VB_{Pre\ OLED}$
V_{OLED}
Node 244
646
VCM
648
VCM_{Pre}
VCM_{RD}
VCM_{Pre}
V_{out}
650
Precharge
652
Integrate
654
Read
656

FIG. 6C

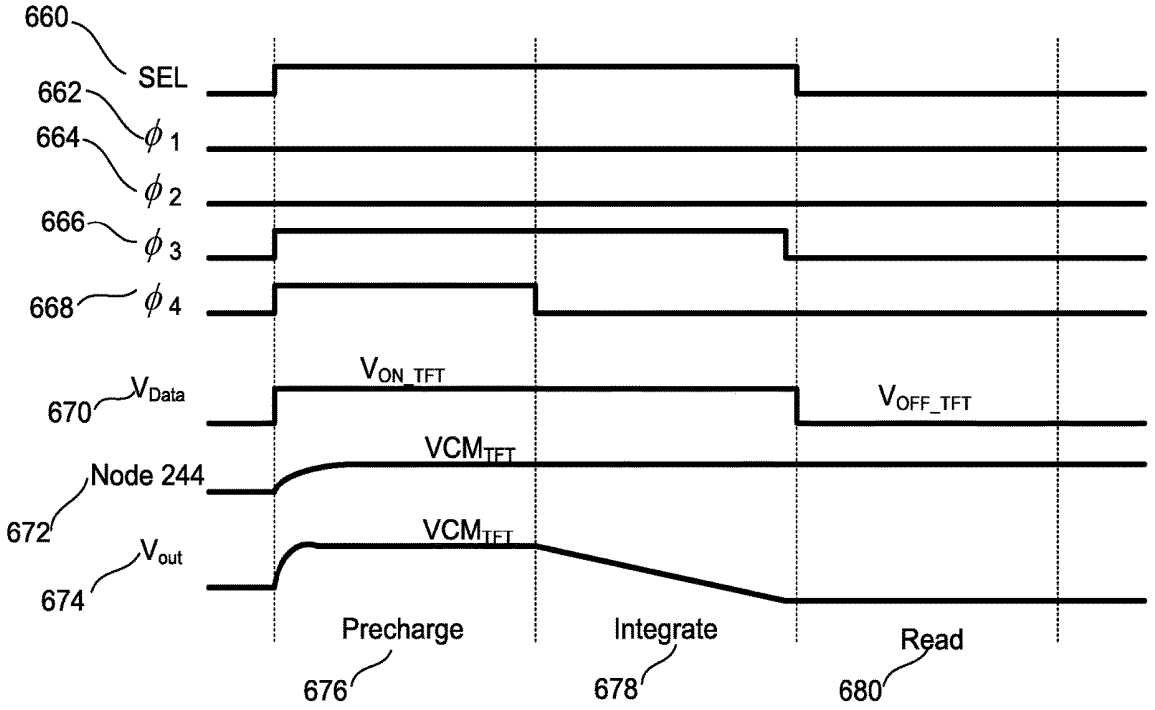

660
SEL
662
ϕ_1
664
ϕ_2
666
ϕ_3
668
ϕ_4
670
V_{Data}
V_{ON_TFT}
V_{OFF_TFT}
VCM_{TFT}
Node 244
672
VCM_{TFT}
V_{out}
674
Precharge
676
Integrate
678
Read
680

FIG. 6D

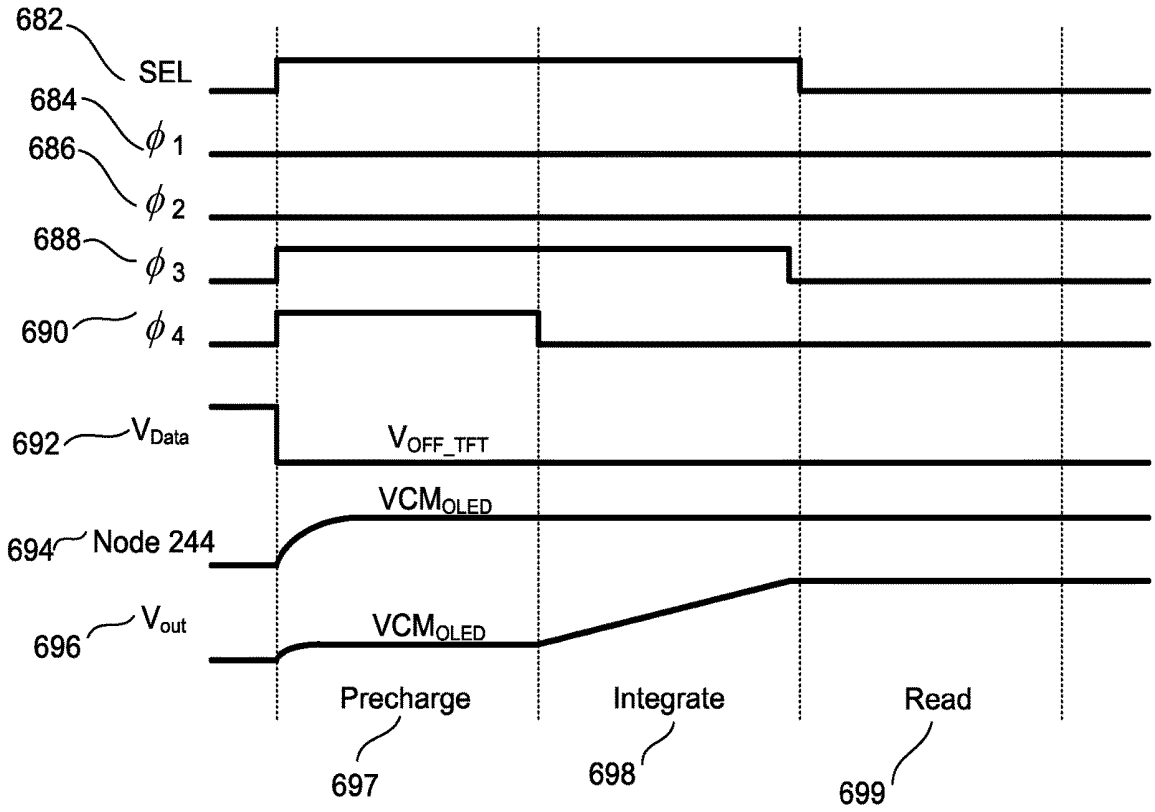

682
SEL
684
ϕ_1
686
ϕ_2
688
ϕ_3
690
ϕ_4
692
V_{Data}
V_{OFF_TFT}
VCM_{OLED}
694
Node 244
696
V_{out}
VCM_{OLED}
Precharge
Integrate
Read
697
698
699

FIG. 7

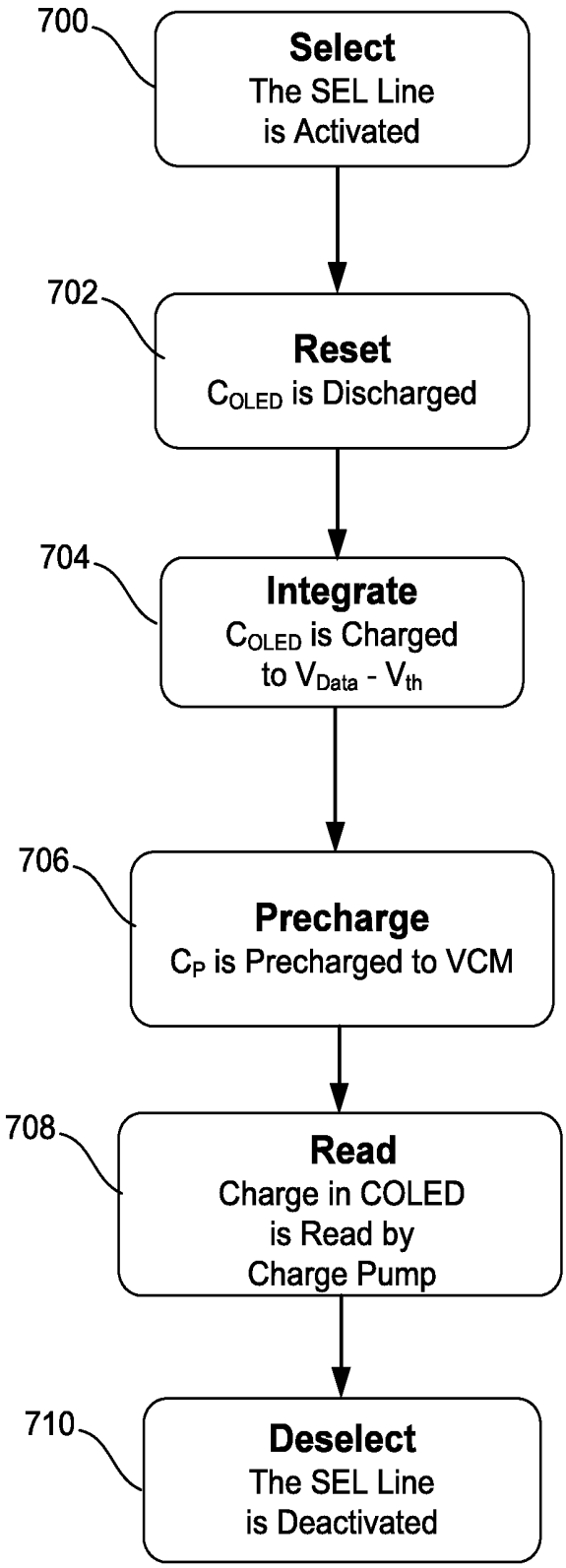

700
Select
The SEL Line
is Activated
702
Reset
C_{OLED} is Discharged
704
Integrate
C_{OLED} is Charged
to V_{Data} - V_{th}
706
Precharge
C_P is Precharged to VCM
708
Read
Charge in COLED
is Read by
Charge Pump
710
Deselect
The SEL Line
is Deactivated

FIG. 8

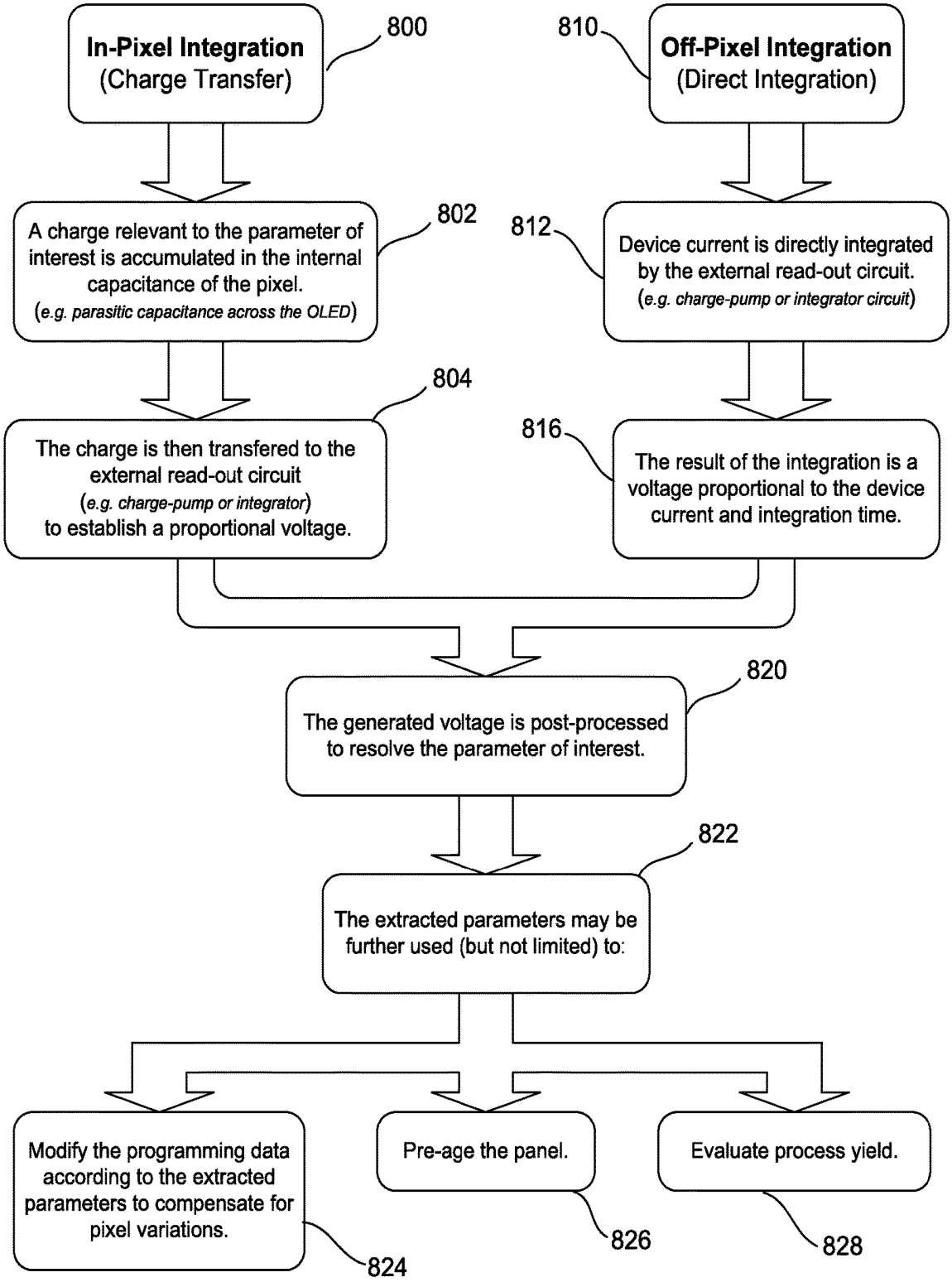
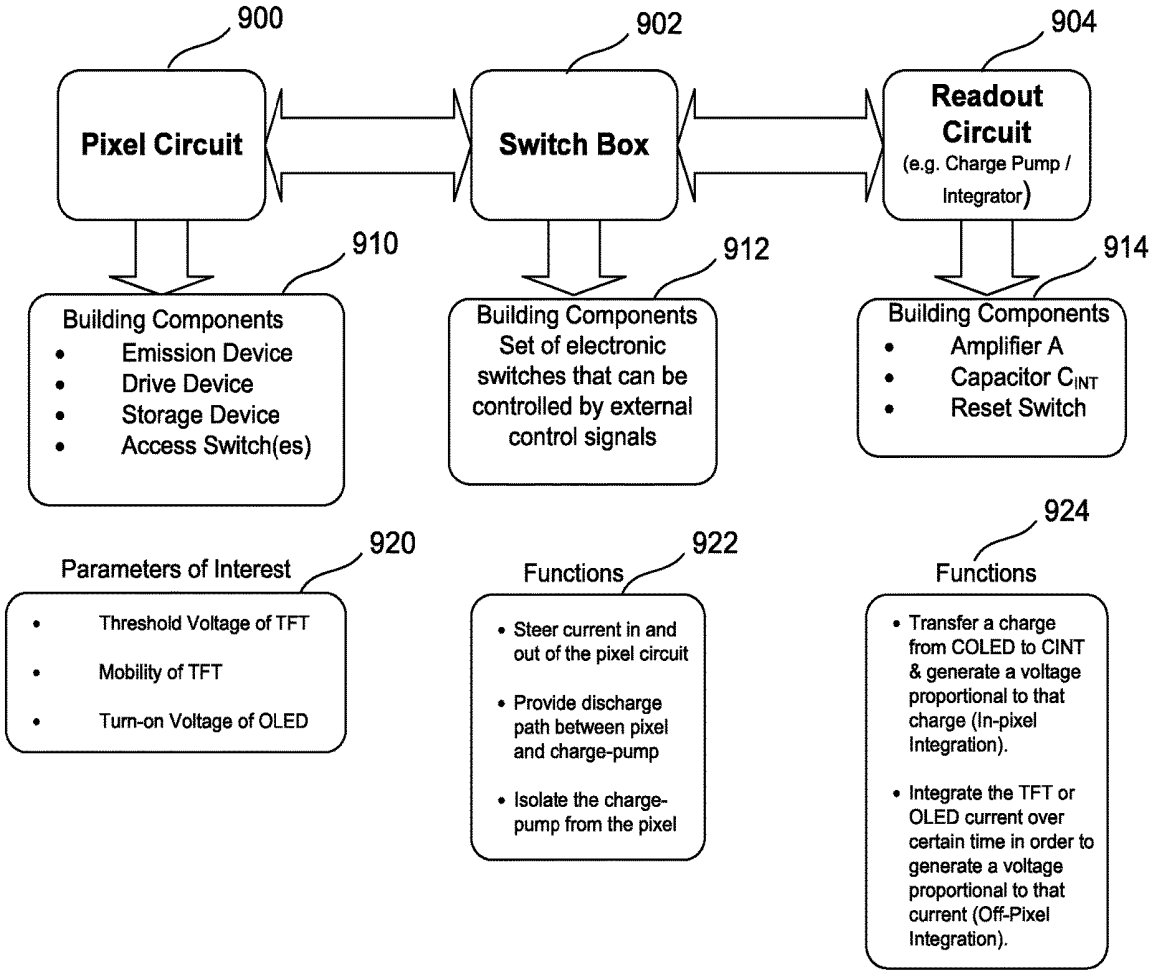

In-Pixel Integration
(Charge Transfer)
800
Off-Pixel Integration
(Direct Integration)
810
A charge relevant to the parameter of interest is accumulated in the internal capacitance of the pixel.
(e.g. parasitic capacitance across the OLED)
802
Device current is directly integrated by the external read-out circuit.
(e.g. charge-pump or integrator circuit)
812
The charge is then transfered to the external read-out circuit
(e.g. charge-pump or integrator)
to establish a proportional voltage.
804
The result of the integration is a voltage proportional to the device current and integration time.
816
The generated voltage is post-processed to resolve the parameter of interest.
820
The extracted parameters may be further used (but not limited) to:
822
Modify the programming data according to the extracted parameters to compensate for pixel variations.
824
Pre-age the panel.
826
Evaluate process yield.
828

FIG. 9


900
902
904
Pixel Circuit
Switch Box
Readout Circuit
(e.g. Charge Pump / Integrator)
910
912
914
Building Components
• Emission Device
• Drive Device
• Storage Device
• Access Switch(es)
Building Components
Set of electronic switches that can be controlled by external control signals
Building Components
• Amplifier A
• Capacitor C_{INT}
• Reset Switch
920
922
924
Parameters of Interest
• Threshold Voltage of TFT
• Mobility of TFT
• Turn-on Voltage of OLED
Functions
• Steer current in and out of the pixel circuit
• Provide discharge path between pixel and charge-pump
• Isolate the charge-pump from the pixel
Functions
• Transfer a charge from COLED to CINT & generate a voltage proportional to that charge (In-pixel Integration).
• Integrate the TFT or OLED current over certain time in order to generate a voltage proportional to that current (Off-Pixel Integration).

SYSTEM AND METHODS FOR EXTRACTION OF THRESHOLD AND MOBILITY PARAMETERS IN AMOLED DISPLAYS

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of, and claims priority to U.S. patent application Ser. No. 15/708,361, filed Sep. 19, 2017, now allowed, which is a continuation of U.S. patent application Ser. No. 15/420,503, filed Jan. 31, 2017, now U.S. Pat. No. 9,799,248, which is a continuation of U.S. patent application Ser. No. 15/154,445, filed May 13, 2016, now U.S. Pat. No. 9,589,490, which is a continuation of U.S. patent application Ser. No. 14/680,554, filed Apr. 7, 2015, now U.S. Pat. No. 9,355,584, which is a continuation of U.S. patent application Ser. No. 13/950,795, filed Jul. 25, 2013, now U.S. Pat. No. 9,093,029, which is a continuation of U.S. patent application Ser. No. 13/112,468, filed May 20, 2011, now U.S. Pat. No. 8,476,217, each of which is hereby incorporated by reference herein in its entirety.

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FIELD OF THE INVENTION

The present invention generally relates to active matrix organic light emitting device (AMOLED) displays, and particularly extracting threshold and mobility factors from the pixel drivers for such displays.

BACKGROUND

Currently, active matrix organic light emitting device ("AMOLED") displays are being introduced. The advantages of such displays include lower power consumption, manufacturing flexibility and faster refresh rate over conventional liquid crystal displays. In contrast to conventional liquid crystal displays, there is no backlighting in an AMOLED display, and thus each pixel consists of different colored OLEDs emitting light independently. The OLEDs emit light based on current supplied through a drive transistor controlled by a programming voltage. The power consumed in each pixel has a relation with the magnitude of the generated light in that pixel.

The quality of output in an OLED based pixel is affected by the properties of the drive transistor, which is typically fabricated from materials including but not limited to amorphous silicon, polysilicon, or metal oxide, as well as the OLED itself. In particular, threshold voltage and mobility of the drive transistor tend to change as the pixel ages. In order to maintain image quality, changes in these parameters must be compensated for by adjusting the programming voltage. In order to do so, such parameters must be extracted from the driver circuit. The addition of components to extract such parameters in a simple driver circuit requires more space on a display substrate for the drive circuitry and thereby reduces the amount of aperture or area of light emission from the OLED.

When biased in saturation, the I-V characteristic of a thin film drive transistor depends on mobility and threshold voltage which are a function of the materials used to fabricate the transistor. Thus different thin film transistor devices implemented across the display panel may demonstrate non-uniform behavior due to aging and process variations in mobility and threshold voltage. Accordingly, for a constant voltage, each device may have a different drain current. An extreme example may be where one device could have low threshold-voltage and low mobility compared to a second device with high threshold-voltage and high mobility.

Thus with very few electronic components available to maintain a desired aperture, extraction of non-uniformity parameters (i.e. threshold voltage, V_{th}, and mobility, μ) of the drive TFT and the OLED becomes challenging. It would be desirable to extract such parameters in a driver circuit for an OLED pixel with as few components as possible to maximize pixel aperture.

SUMMARY

One example disclosed is a data extraction system for an organic light emitting device (OLED) based display. The system includes a pixel circuit including an organic light emitting device, a drive device to provide a programmable drive current to the light emitting device, a programming input to provide a programming signal, and a storage device to store the programming signal. A charge-pump amplifier has a current input and a voltage output. The charge-pump amplifier includes an operational amplifier in negative feedback configuration. The feedback is provided by a capacitor connected between the output and the inverting input of the operational amplifier. A common-mode voltage source drives the non-inverting input of the operational amplifier. An electronic switch is coupled across the capacitor to reset the capacitor. A switch module including the input is coupled to the output of the pixel circuit and an output is coupled to the input of the charge-pump amplifier. The switch module includes a plurality of electronic switches that may be controlled by external control signals to steer current in and out of the pixel circuit, provide a discharge path between the pixel circuit and the charge-pump amplifier and isolate the charge-pump amplifier from the pixel circuit. A controller is coupled to the pixel circuit, charge-pump amplifier and the switch module. The controller controls input signals to the pixel circuit, charge-pump amplifier and switch module in a predetermined sequence to produce an output voltage value which is a function of a parameter of the pixel circuit. The sequence includes providing a program voltage to the programming input to either pre-charge an internal capacitance of the pixel circuit to a charge level and transfer the charge to the charge-pump amplifier via the switch module to generate the output voltage value or provide a current from the pixel circuit to the charge-pump amplifier via the switch module to produce the output voltage value by integration over a certain period of time.

Another example is a method of extracting a circuit parameter from a pixel circuit including an organic light emitting device, a drive device to provide a programmable drive current to the light emitting device, a programming input, and a storage device to store a programming signal. A predetermined program voltage is provided to the programming voltage input. A capacitance of the pixel circuit is

charged to a charge level or a current from the pixel circuit. The pixel circuit is coupled to a charge-pump amplifier. The charge-pump amplifier is isolated from the pixel circuit to provide a voltage output either proportional to the charge level or to integrate the current from the pixel circuit. The voltage output of the charge-pump amplifier is read. At least one pixel circuit parameter is determined from the voltage output of the charge-pump amplifier.

Another example is a data extraction system for an organic light emitting device (OLED) based display. The system includes a pixel circuit having a drive transistor, an organic light emitting device, and a programming input coupled to the gate of the drive transistor. The drive transistor has a source or a drain coupled to the OLED. A charge-pump amplifier has an input and an integrated voltage output. A switch module includes an input coupled to the output of the pixel circuit and an output coupled to the input of the charge-pump amplifier. The switch module includes switches to steer current in and out of the pixel circuit, provide a discharge path between the pixel circuit and the charge-pump amplifier and isolate the charge-pump amplifier from the pixel circuit. A controller is coupled to the pixel circuit, charge-pump amplifier and the switch module. The controller controls voltage inputs to the pixel circuit, charge-pump amplifier and switch module in a predetermined sequence to produce an output voltage value which is a function of a parameter of the pixel circuit. The sequence including providing a program voltage to the programming input to either pre-charge a capacitance of the pixel circuit to a charge level, transfer the charge to the charge-pump amplifier via the switch module to generate the output voltage value or provide a current from the pixel circuit to the charge-pump amplifier via the switch module to produce the output voltage value by integration.

The foregoing and additional aspects and embodiments of the present invention will be apparent to those of ordinary skill in the art in view of the detailed description of various embodiments and/or aspects, which is made with reference to the drawings, a brief description of which is provided next.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings.

FIG. **1** is a block diagram of an AMOLED display with compensation control;

FIG. **2** is a circuit diagram of a data extraction circuit for a two-transistor pixel in the AMOLED display in FIG. **1**;

FIG. **3**A is a signal timing diagram of the signals to the data extraction circuit to extract the threshold voltage and mobility of an n-type drive transistor in FIG. **2**;

FIG. **3**B is a signal timing diagram of the signals to the data extraction circuit to extract the characteristic voltage of the OLED in FIG. **2** with an n-type drive transistor;

FIG. **3**C is a signal timing diagram of the signals to the data extraction circuit for a direct read to extract the threshold voltage of an n-type drive transistor in FIG. **2**;

FIG. **4**A is a signal timing diagram of the signals to the data extraction circuit to extract the threshold voltage and mobility of a p-type drive transistor in FIG. **2**;

FIG. **4**B is a signal timing diagram of the signals to the data extraction circuit to extract the characteristic voltage of the OLED in FIG. **2** with a p-type drive transistor;

FIG. **4**C is a signal timing diagram of the signals to the data extraction circuit for a direct read to extract the threshold voltage of a p-type drive transistor in FIG. **2**;

FIG. **4**D is a signal timing diagram of the signals to the data extraction circuit for a direct read of the OLED turn-on voltage using either an n-type or p-type drive transistor in FIG. **2**.

FIG. **5** is a circuit diagram of a data extraction circuit for a three-transistor drive circuit for a pixel in the AMOLED display in FIG. **1** for extraction of parameters;

FIG. **6**A is a signal timing diagram of the signals to the data extraction circuit to extract the threshold voltage and mobility of the drive transistor in FIG. **5**;

FIG. **6**B is a signal timing diagram of the signals to the data extraction circuit to extract the characteristic voltage of the OLED in FIG. **5**;

FIG. **6**C is a signal timing diagram the signals to the data extraction circuit for a direct read to extract the threshold voltage of the drive transistor in FIG. **5**;

FIG. **6**D is a signal timing diagram of the signals to the data extraction circuit for a direct read to extract the characteristic voltage of the OLED in FIG. **5**;

FIG. **7** is a flow diagram of the extraction cycle to readout the characteristics of the drive transistor and the OLED of a pixel circuit in an AMOLED display;

FIG. **8** is a flow diagram of different parameter extraction cycles and final applications; and

FIG. **9** is a block diagram and chart of the components of a data extraction system.

While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and will be described in detail herein. It should be understood, however, that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION

FIG. **1** is an electronic display system **100** having an active matrix area or pixel array **102** in which an n×m array of pixels **104** are arranged in a row and column configuration. For ease of illustration, only two rows and two columns are shown. External to the active matrix area of the pixel array **102** is a peripheral area **106** where peripheral circuitry for driving and controlling the pixel array **102** are disposed. The peripheral circuitry includes an address or gate driver circuit **108**, a data or source driver circuit **110**, a controller **112**, and an optional supply voltage (e.g., Vdd) driver **114**. The controller **112** controls the gate, source, and supply voltage drivers **108**, **110**, **114**. The gate driver **108**, under control of the controller **112**, operates on address or select lines SEL[i], SEL[i+1], and so forth, one for each row of pixels **104** in the pixel array **102**. In pixel sharing configurations described below, the gate or address driver circuit **108** can also optionally operate on global select lines GSEL [j] and optionally/GSEL[j], which operate on multiple rows of pixels **104** in the pixel array **102**, such as every two rows of pixels **104**. The source driver circuit **110**, under control of the controller **112**, operates on voltage data lines Vdata[k], Vdata[k+1], and so forth, one for each column of pixels **104** in the pixel array **102**. The voltage data lines carry voltage programming information to each pixel **104** indicative of the brightness of each light emitting device in the pixel **104**. A storage element, such as a capacitor, in each pixel **104** stores

the voltage programming information until an emission or driving cycle turns on the light emitting device. The optional supply voltage driver **114**, under control of the controller **112**, controls a supply voltage (EL_Vdd) line, one for each row or column of pixels **104** in the pixel array **102**.

The display system **100** further includes a current supply and readout circuit **120**, which reads output data from data output lines, VD [k], VD [k+1], and so forth, one for each column of pixels **104** in the pixel array **102**.

As is known, each pixel **104** in the display system **100** needs to be programmed with information indicating the brightness of the light emitting device in the pixel **104**. A frame defines the time period that includes: (i) a programming cycle or phase during which each and every pixel in the display system **100** is programmed with a programming voltage indicative of a brightness; and (ii) a driving or emission cycle or phase during which each light emitting device in each pixel is turned on to emit light at a brightness commensurate with the programming voltage stored in a storage element. A frame is thus one of many still images that compose a complete moving picture displayed on the display system **100**. There are at least schemes for programming and driving the pixels: row-by-row, or frame-by-frame. In row-by-row programming, a row of pixels is programmed and then driven before the next row of pixels is programmed and driven. In frame-by-frame programming, all rows of pixels in the display system **100** are programmed first, and all rows of pixels are driven at once. Either scheme can employ a brief vertical blanking time at the beginning or end of each frame during which the pixels are neither programmed nor driven.

The components located outside of the pixel array **102** may be disposed in a peripheral area **106** around the pixel array **102** on the same physical substrate on which the pixel array **102** is disposed. These components include the gate driver **108**, the source driver **110**, the optional supply voltage driver **114**, and a current supply and readout circuit **120**. Alternately, some of the components in the peripheral area **106** may be disposed on the same substrate as the pixel array **102** while other components are disposed on a different substrate, or all of the components in the peripheral area can be disposed on a substrate different from the substrate on which the pixel array **102** is disposed. Together, the gate driver **108**, the source driver **110**, and the supply voltage driver **114** make up a display driver circuit. The display driver circuit in some configurations can include the gate driver **108** and the source driver **110** but not the supply voltage control **114**.

When biased in saturation, the first order I-V characteristic of a metal oxide semiconductor (MOS) transistor (a thin film transistor in this case of interest) is modeled as:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

where I_D is the drain current and V_{GS} is the voltage difference applied between gate and source terminals of the transistor. The thin film transistor devices implemented across the display system **100** demonstrate non-uniform behavior due to aging and process variations in mobility (μ) and threshold voltage (V_{th}). Accordingly, for a constant voltage difference applied between gate and source, V_{GS}, each transistor on the pixel matrix **102** may have a different drain current based on a non-deterministic mobility and threshold voltage:

$$I_{D(i,j)} = f(\mu_{i,j}, V_{th\ i,j})$$

where i and j are the coordinates (row and column) of a pixel in an n×m array of pixels such as the array of pixels **102** in FIG. **1**.

FIG. **2** shows a data extraction system **200** including a two-transistor (2T) driver circuit **202** and a readout circuit **204**. The supply voltage control **114** is optional in a display system with 2T pixel circuit **104**. The readout circuit **204** is part of the current supply and readout circuit **120** and gathers data from a column of pixels **104** as shown in FIG. **1**. The readout circuit **204** includes a charge pump circuit **206** and a switch-box circuit **208**. A voltage source **210** provides the supply voltage to the driver circuit **202** through the switch-box circuit **208**. The charge-pump and switch-box circuits **206** and **208** are implemented on the top or bottom side of the array **102** such as in the voltage drive **114** and the current supply and readout circuit **120** in FIG. **1**. This is achieved by either direct fabrication on the same substrate as the pixel array **102** or by bonding a microchip on the substrate or a flex as a hybrid solution.

The driver circuit **202** includes a drive transistor **220**, an organic light emitting device **222**, a drain storage capacitor **224**, a source storage capacitor **226**, and a select transistor **228**. A supply line **212** provides the supply voltage and also a monitor path (for the readout circuit **204**) to a column of driver circuits such as the driver circuit **202**. A select line input **230** is coupled to the gate of the select transistor **228**. A programming data input **232** is coupled to the gate of the drive transistor **220** through the select transistor **228**. The drain of the drive transistor **220** is coupled to the supply voltage line **212** and the source of the drive transistor **220** is coupled to the OLED **222**. The select transistor **228** controls the coupling of the programming input **230** to the gate of the drive transistor **220**. The source storage capacitor **226** is coupled between the gate and the source of the drive transistor **220**. The drain storage capacitor **224** is coupled between the gate and the drain of the drive transistor **220**. The OLED **222** has a parasitic capacitance that is modeled as a capacitor **240**. The supply voltage line **212** also has a parasitic capacitance that is modeled as a capacitor **242**. The drive transistor **220** in this example is a thin film transistor that is fabricated from amorphous silicon. Of course other materials such as polysilicon or metal oxide may be used. A node **244** is the circuit node where the source of the drive transistor **220** and the anode of the OLED **222** are coupled together. In this example, the drive transistor **220** is an n-type transistor. The system **200** may be used with a p-type drive transistor in place of the n-type drive transistor **220** as will be explained below.

The readout circuit **204** includes the charge-pump circuit **206** and the switch-box circuit **208**. The charge-pump circuit **206** includes an amplifier **250** having a positive and negative input. The negative input of the amplifier **250** is coupled to a capacitor **252** (C_{int}) in parallel with a switch **254** in a negative feedback loop to an output **256** of the amplifier **250**. The switch **254** (S4) is utilized to discharge the capacitor **252** C_{int} during the pre-charge phase. The positive input of the amplifier **250** is coupled to a common mode voltage input **258** (VCM). The output **256** of the amplifier **250** is indicative of various extracted parameters of the drive transistor **220** and OLED **222** as will be explained below.

The switch-box circuit **208** includes several switches **260**, **262** and **264** (S1, S2 and S3) to steer current to and from the pixel driver circuit **202**. The switch **260** (S1) is used during the reset phase to provide a discharge path to ground. The switch **262** (S2) provides the supply connection during

normal operation of the pixel **104** and also during the integration phase of readout. The switch **264** (S3) is used to isolate the charge-pump circuit **206** from the supply line voltage **212** (VD).

The general readout concept for the two transistor pixel driver circuit **202** for each of the pixels **104**, as shown in FIG. **2**, comes from the fact that the charge stored on the parasitic capacitance represented by the capacitor **240** across the OLED **222** has useful information of the threshold voltage and mobility of the drive transistor **220** and the turn-on voltage of the OLED **222**. The extraction of such parameters may be used for various applications. For example, such parameters may be used to modify the programming data for the pixels **104** to compensate for pixel variations and maintain image quality. Such parameters may also be used to pre-age the pixel array **102**. The parameters may also be used to evaluate the process yield for the fabrication of the pixel array **102**.

Assuming that the capacitor **240** (C_{OLED}) is initially discharged, it takes some time for the capacitor **240** (C_{OLED}) to charge up to a voltage level that turns the drive transistor **220** off. This voltage level is a function of the threshold voltage of the drive transistor **220**. The voltage applied to the programming data input **232** (V_{Data}) must be low enough such that the settled voltage of the OLED **222** (V_{OLED}) is less than the turn-on threshold voltage of the OLED **222** itself. In this condition, $V_{Data}-V_{OLED}$ is a linear function of the threshold voltage (V_{th}) of the drive transistor **220**. In order to extract the mobility of a thin film transistor device such as the drive transistor **220**, the transient settling of such devices, which is a function of both the threshold voltage and mobility, is considered. Assuming that the threshold voltage deviation among the TFT devices such as the drive transistor **220** is compensated, the voltage of the node **244** sampled at a constant interval after the beginning of integration is a function of mobility only of the TFT device such as the drive transistor **220** of interest.

FIG. **3**A-**3**C are signal timing diagrams of the control signals applied to the components in FIG. **2** to extract parameters such as voltage threshold and mobility from the drive transistor **220** and the turn on voltage of the OLED **222** in the drive circuit **200** assuming the drive transistor **220** is an n-type transistor. Such control signals could be applied by the controller **112** to the source driver **110**, the gate driver **108** and the current supply and readout circuit **120** in FIG. **1**. FIG. **3**A is a timing diagram showing the signals applied to the extraction circuit **200** to extract the threshold voltage and mobility from the drive transistor **220**. FIG. **3**A includes a signal **302** for the select input **230** in FIG. **2**, a signal **304** (ϕ_1) to the switch **260**, a signal **306** (ϕ_2) for the switch **262**, a signal **308** (ϕ_3) for the switch **264**, a signal **310** (ϕ_4) for the switch **254**, a programming voltage signal **312** for the programming data input **232** in FIG. **2**, a voltage **314** of the node **244** in FIG. **2** and an output voltage signal **316** for the output **256** of the amplifier **250** in FIG. **2**.

FIG. **3**A shows the four phases of the readout process, a reset phase **320**, an integration phase **322**, a pre-charge phase **324** and a read phase **326**. The process starts by activating a high select signal **302** to the select input **230**. The select signal **302** will be kept high throughout the readout process as shown in FIG. **3**A.

During the reset phase **320**, the input signal **304** (ϕ_1) to the switch **260** is set high in order to provide a discharge path to ground. The signals **306**, **308** and **310** (ϕ_2, ϕ_3, ϕ_4) to the switches **262**, **264** and **250** are kept low in this phase. A high enough voltage level (V_{RST_TFT}) is applied to the programming data input **232** (V_{Data}) to maximize the current flow through the drive transistor **220**. Consequently, the voltage at the node **244** in FIG. **2** is discharged to ground to get ready for the next cycle.

During the integration phase **322**, the signal **304** (ϕ_2) to the switch **262** stays high which provides a charging path from the voltage source **210** through the switch **262**. The signals **304**, **308** and **310** (ϕ_1, ϕ_3, ϕ_4) to the switches **260**, **264** and **250** are kept low in this phase. The programming voltage input **232** (V_{Data}) is set to a voltage level (V_{INT_TFT}) such that once the capacitor **240** (C_{oled}) is fully charged, the voltage at the node **244** is less than the turn-on voltage of the OLED **222**. This condition will minimize any interference from the OLED **222** during the reading of the drive transistor **220**. Right before the end of integration time, the signal **312** to the programming voltage input **232** (V_{Data}) is lowered to V_{OFF} in order to isolate the charge on the capacitor **240** (C_{oled}) from the rest of the circuit.

When the integration time is long enough, the charge stored on capacitor **240** (C_{oled}) will be a function of the threshold voltage of the drive transistor **220**. For a shortened integration time, the voltage at the node **244** will experience an incomplete settling and the stored charge on the capacitor **240** (C_{oled}) will be a function of both the threshold voltage and mobility of the drive transistor **220**. Accordingly, it is feasible to extract both parameters by taking two separate readings with short and long integration phases.

During the pre-charge phase **324**, the signals **304** and **306** (ϕ_1, ϕ_2) to switches **260** and **262** are set low. Once the input signal **310** (ϕ_4) to the switch **254** is set high, the amplifier **250** is set in a unity feedback configuration. In order to protect the output stage of the amplifier **250** against short-circuit current from the supply voltage **210**, the signal **308** (ϕ_3) to the switch **264** goes high when the signal **306** (ϕ_2) to the switch **262** is set low. When the switch **264** is closed, the parasitic capacitance **242** of the supply line is precharged to the common mode voltage, VCM. The common mode voltage, VCM, is a voltage level which must be lower than the ON voltage of the OLED **222**. Right before the end of pre-charge phase, the signal **310** (ϕ_4) to the switch **254** is set low to prepare the charge pump amplifier **250** for the read cycle.

During the read phase **336**, the signals **304**, **306** and **310** (ϕ_1, ϕ_2, ϕ_4) to the switches **260**, **262** and **254** are set low. The signal **308** (ϕ_3) to the switch **264** is kept high to provide a charge transfer path from the drive circuit **202** to the charge-pump amplifier **250**. A high enough voltage **312** (V_{RA_TFT}) is applied to the programming voltage input **232** (V_{Data}) to minimize the channel resistance of the drive transistor **220**. If the integration cycle is long enough, the accumulated charge on the capacitor **252** (C_{int}) is not a function of integration time. Accordingly, the output voltage of the charge-pump amplifier **250** in this case is equal to:

$$V_{out} = -\frac{C_{oled}}{C_{int}}(V_{Data} - V_{th})$$

For a shortened integration time, the accumulated charge on the capacitor **252** (C_{int}) is given by:

$$Q_{int} = \int^{T_{int}} i_D(V_{GS}, V_{th}, \mu) \cdot dt$$

Consequently, the output voltage **256** of the charge-pump amplifier **250** at the end of read cycle equals:

$$V_{out} = -\frac{1}{C_{int}} \cdot \int^{T_{int}} i_D(V_{GS}, V_{th}, \mu) \cdot dt$$

Hence, the threshold voltage and the mobility of the drive transistor **220** may be extracted by reading the output voltage **256** of the amplifier **250** in the middle and at the end of the read phase **326**.

FIG. **3**B is a timing diagram for the reading process of the threshold turn-on voltage parameter of the OLED **222** in FIG. **2**. The reading process of the OLED **222** also includes four phases, a reset phase **340**, an integration phase **342**, a pre-charge phase **344** and a read phase **346**. Just like the reading process for the drive transistor **220** in FIG. **3**A, the reading process for OLED starts by activating the select input **230** with a high select signal **302**. The timing of the signals **304**, **306**, **308**, and **310** (ϕ_1, ϕ_2, ϕ_3, ϕ_4) to the switches **260**, **262**, **264** and **254** is the same as the read process for the drive transistor **220** in FIG. **3**A. A programming signal **332** for the programming input **232**, a signal **334** for the node **244** and an output signal **336** for the output of the amplifier **250** are different from the signals in FIG. **3**A.

During the reset phase **340**, a high enough voltage level **332** (V_{RST_OLED}) is applied to the programming data input **232** (V_{Data}) to maximize the current flow through the drive transistor **220**. Consequently, the voltage at the node **244** in FIG. **2** is discharged to ground through the switch **260** to get ready for the next cycle.

During the integration phase **342**, the signal **306** (ϕ_2) to the switch **262** stays high which provides a charging path from the voltage source **210** through the switch **262**. The programming voltage input **232** (V_{Data}) is set to a voltage level **332** (V_{INT_OLED}) such that once the capacitor **240** (C_{oled}) is fully charged, the voltage at the node **244** is greater than the turn-on voltage of the OLED **222**. In this case, by the end of the integration phase **342**, the drive transistor **220** is driving a constant current through the OLED **222**.

During the pre-charge phase **344**, the drive transistor **220** is turned off by the signal **332** to the programming input **232**. The capacitor **240** (C_{oled}) is allowed to discharge until it reaches the turn-on voltage of OLED **222** by the end of the pre-charge phase **344**.

During the read phase **346**, a high enough voltage **332** (V_{RD_OLED}) is applied to the programming voltage input **232** (V_{Data}) to minimize the channel resistance of the drive transistor **220**. If the pre-charge phase is long enough, the settled voltage across the capacitor **252** (C_{int}) will not be a function of pre-charge time. Consequently, the output voltage **256** of the charge-pump amplifier **250** at the end of the read phase is given by:

$$V_{out} = -\frac{C_{oled}}{C_{int}} \cdot V_{ON,oled}$$

The signal **308** (ϕ_3) to the switch **264** is kept high to provide a charge transfer path from the drive circuit **202** to the charge-pump amplifier **250**. Thus the output voltage signal **336** may be used to determine the turn-on voltage of the OLED **220**.

FIG. **3**C is a timing diagram for the direct reading of the drive transistor **220** using the extraction circuit **200** in FIG. **2**. The direct reading process has a reset phase **350**, a pre-charge phase **352** and an integrate/read phase **354**. The readout process is initiated by activating the select input **230** in FIG. **2**. The select signal **302** to the select input **230** is kept high throughout the readout process as shown in FIG. **3**C. The signals **364** and **366** (ϕ_1, ϕ_2) for the switches **260** and **262** are inactive in this readout process.

During the reset phase **350**, the signals **368** and **370** (ϕ_3, ϕ_4) for the switches **264** and **254** are set high in order to provide a discharge path to virtual ground. A high enough voltage **372** (V_{RST_TFT}) is applied to the programming input **232** (V_{Data}) to maximize the current flow through the drive transistor **220**. Consequently, the node **244** is discharged to the common-mode voltage **374** (VCM_{RST}) to get ready for the next cycle.

During the pre-charge phase **354**, the drive transistor **220** is turned off by applying an off voltage **372** (V_{OFF}) to the programming input **232** in FIG. **2**. The common-mode voltage input **258** to the positive input of the amplifier **250** is raised to VCM_{RD} in order to precharge the line capacitance. At the end of the pre-charge phase **354**, the signal **370** (ϕ_4) to the switch **254** is turned off to prepare the charge-pump amplifier **250** for the next cycle.

At the beginning of the read/integrate phase **356**, the programming voltage input **232** (V_{Data}) is raised to V_{INT_TFT} **372** to turn the drive transistor **220** on. The capacitor **240** (C_{OLED}) starts to accumulate the charge until V_{Data} minus the voltage at the node **244** is equal to the threshold voltage of the drive transistor **220**. In the meantime, a proportional charge is accumulated in the capacitor **252** (C_{INT}). Accordingly, at the end of the read cycle **356**, the output voltage **376** at the output **256** of the amplifier **250** is a function of the threshold voltage which is given by:

$$V_{out} = \frac{C_{oled}}{C_{int}} \cdot (V_{Data} - V_{th})$$

As indicated by the above equation, in the case of the direct reading, the output voltage has a positive polarity. Thus, the threshold voltage of the drive transistor **220** may be determined by the output voltage of the amplifier **250**.

As explained above, the drive transistor **220** in FIG. **2** may be a p-type transistor. FIG. **4**A-**4**C are signal timing diagrams of the signals applied to the components in FIG. **2** to extract voltage threshold and mobility from the drive transistor **220** and the OLED **222** when the drive transistor **220** is a p-type transistor. In the example where the drive transistor **220** is a p-type transistor, the source of the drive transistor **220** is coupled to the supply line **212** (VD) and the drain of the drive transistor **220** is coupled to the OLED **222**. FIG. **4**A is a timing diagram showing the signals applied to the extraction circuit **200** to extract the threshold voltage and mobility from the drive transistor **220** when the drive transistor **220** is a p-type transistor. FIG. **4**A shows voltage signals **402**-**416** for the select input **232**, the switches **260**, **262**, **264** and **254**, the programming data input **230**, the voltage at the node **244** and the output voltage **256** in FIG. **2**. The data extraction is performed in three phases, a reset phase **420**, an integrate/pre-charge phase **422**, and a read phase **424**.

As shown in FIG. **4**A, the select signal **402** is active low and kept low throughout the readout phases **420**, **422** and **424**. Throughout the readout process, the signals **404** and **406** (ϕ_1, ϕ_2) to the switches **260** and **262** are kept low (inactive). During the reset phase, the signals **408** and **410** (ϕ_3, ϕ_4) at the switches **264** and **254** are set to high in order to charge the node **244** to a reset common mode voltage level VCM_{rst}. The common-mode voltage input **258** on the charge-pump input **258** (VCM_{rst}) should be low enough to

keep the OLED **222** off. The programming data input **232** V_{Data} is set to a low enough value **412** (V_{RST_TFT}) to provide maximum charging current through the driver transistor **220**.

During the integrate/pre-charge phase **422**, the common-mode voltage on the common voltage input **258** is reduced to VCM_{int} and the programming input **232** (V_{Data}) is increased to a level **412** (V_{INT_TFT}) such that the drive transistor **220** will conduct in the reverse direction. If the allocated time for this phase is long enough, the voltage at the node **244** will decline until the gate to source voltage of the drive transistor **220** reaches the threshold voltage of the drive transistor **220**. Before the end of this cycle, the signal **410** (ϕ_4) to the switch **254** goes low in order to prepare the charge-pump amplifier **250** for the read phase **424**.

The read phase **424** is initiated by decreasing the signal **412** at the programming input **232** (V_{Data}) to V_{RD_TFT} so as to turn the drive transistor **220** on. The charge stored on the capacitor **240** (C_{OLED}) is now transferred to the capacitor **254** (C_{INT}). At the end of the read phase **424**, the signal **408** (ϕ_3) to the switch **264** is set to low in order to isolate the charge-pump amplifier **250** from the drive circuit **202**. The output voltage signal **416** V_{out} from the amplifier output **256** is now a function of the threshold voltage of the drive transistor **220** given by:

$$V_{out} = -\frac{C_{oled}}{C_{int}} \cdot (V_{INT\_TFT} - V_{th})$$

FIG. **4**B is a timing diagram for the in-pixel extraction of the threshold voltage of the OLED **222** in FIG. **2** assuming that the drive transistor **220** is a p-type transistor. The extraction process is very similar to the timing of signals to the extraction circuit **200** for an n-type drive transistor in FIG. **3**A. FIG. **4**B shows voltage signals **432-446** for the select input **230**, the switches **260**, **262**, **264** and **254**, the programming data input **232**, the voltage at the node **244** and the amplifier output **256** in FIG. **2**. The extraction process includes a reset phase **450**, an integration phase **452**, a pre-charge phase **454** and a read phase **456**. The major difference in this readout cycle in comparison to the readout cycle in FIG. **4**A is the voltage levels of the signal **442** to the programming data input **232** (V_{Data}) that are applied to the driver circuit **210** in each readout phase. For a p-type thin film transistor that may be used for the drive transistor **220**, the select signal **430** to the select input **232** is active low. The select input **232** is kept low throughout the readout process as shown in FIG. **4**B.

The readout process starts by first resetting the capacitor **240** (C_{OLED}) in the reset phase **450**. The signal **434** (ϕ_1) to the switch **260** is set high to provide a discharge path to ground. The signal **442** to the programming input **232** (V_{Data}) is lowered to V_{RST_OLED} in order to turn the drive transistor **220** on.

In the integrate phase **452**, the signals **434** and **436** (ϕ_1, ϕ_2) to the switches **260** and **262** are set to off and on states respectively, to provide a charging path to the OLED **222**. The capacitor **240** (C_{OLED}) is allowed to charge until the voltage **444** at node **244** goes beyond the threshold voltage of the OLED **222** to turn it on. Before the end of the integration phase **452**, the voltage signal **442** to the programming input **232** (V_{Data}) is raised to V_{OFF} to turn the drive transistor **220** off.

During the pre-charge phase **454**, the accumulated charge on the capacitor **240** (C_{OLED}) is discharged into the OLED **222** until the voltage **444** at the node **244** reaches the threshold voltage of the OLED **222**. Also, in the pre-charge phase **454**, the signals **434** and **436** (ϕ_1, ϕ_2) to the switches **260** and **262** are turned off while the signals **438** and **440** (ϕ_3, ϕ_4) to the switches **264** and **254** are set on. This provides the condition for the amplifier **250** to precharge the supply line **212** (VD) to the common mode voltage input **258** (VCM) provided at the positive input of the amplifier **250**. At the end of the pre-charge phase, the signal **430** (ϕ_4) to the switch **254** is turned off to prepare the charge-pump amplifier **250** for the read phase **456**.

The read phase **456** is initiated by turning the drive transistor **220** on when the voltage **442** to the programming input **232** (V_{Data}) is lowered to V_{RD_OLED}. The charge stored on the capacitor **240** (C_{OLED}) is now transferred to the capacitor **254** (C_{INT}) which builds up the output voltage **446** at the output **256** of the amplifier **250** as a function of the threshold voltage of the OLED **220**.

FIG. **4**C is a signal timing diagram for the direct extraction of the threshold voltage of the drive transistor **220** in the extraction system **200** in FIG. **2** when the drive transistor **220** is a p-type transistor. FIG. **4**C shows voltage signals **462-476** for the select input **230**, the switches **260**, **262**, **264** and **254**, the programming data input **232**, the voltage at the node **244** and the output voltage **256** in FIG. **2**. The extraction process includes a pre-charge phase **480** and an integration phase **482**. However, in the timing diagram in FIG. **4**C, a dedicated final read phase **484** is illustrated which may be eliminated if the output of charge-pump amplifier **250** is sampled at the end of the integrate phase **482**.

The extraction process is initiated by simultaneous pre-charging of the drain storage capacitor **224**, the source storage capacitor **226**, the capacitor **240** (C_{OLED}) and the capacitor **242** in FIG. **2**. For this purpose, the signals **462**, **468** and **470** to the select line input **230** and the switches **264** and **254** are activated as shown in FIG. **4**C. Throughout the readout process, the signals **404** and **406** (ϕ_1, ϕ_2) to the switches **260** and **262** are kept low. The voltage level of common mode voltage input **258** (VCM) determines the voltage on the supply line **212** and hence the voltage at the node **244**. The common mode voltage (VCM) should be low enough such that the OLED **222** does not turn on. The voltage **472** to the programming input **232** (V_{Data}) is set to a level (V_{RST_TFT}) low enough to turn the transistor **220** on.

At the beginning of the integrate phase **482**, the signal **470** (ϕ_4) to the switch **254** is turned off in order to allow the charge-pump amplifier **250** to integrate the current through the drive transistor **220**. The output voltage **256** of the charge-pump amplifier **250** will incline at a constant rate which is a function of the threshold voltage of the drive transistor **220** and its gate-to-source voltage. Before the end of the integrate phase **482**, the signal **468** (ϕ_3) to the switch **264** is turned off to isolate the charge-pump amplifier **250** from the driver circuit **220**. Accordingly, the output voltage **256** of the amplifier **250** is given by:

$$V_{out} = I_{TFT} \cdot \frac{T_{int}}{C_{int}}$$

where I_{TFT} is the drain current of the drive transistor **220** which is a function of the mobility and (V_{CM}–V_{Data}–$|V_{th}|$). T_{int} is the length of the integration time. In the optional read phase **484**, the signal **468** (ϕ_3) to the switch **264** is kept low to isolate the charge-pump amplifier **250** from the driver circuit **202**. The output voltage **256**, which is a function of

the mobility and threshold voltage of the drive transistor **220**, may be sampled any time during the read phase **484**.

FIG. **4**D is a timing diagram for the direct reading of the OLED **222** in FIG. **2**. When the drive transistor **220** is turned on with a high enough gate-to-source voltage it may be utilized as an analog switch to access the anode terminal of the OLED **222**. In this case, the voltage at the node **244** is essentially equal to the voltage on the supply line **212** (VD). Accordingly, the drive current through the drive transistor **220** will only be a function of the turn-on voltage of the OLED **222** and the voltage that is set on the supply line **212**. The drive current may be provided by the charge-pump amplifier **250**. When integrated over a certain time period, the output voltage **256** of the integrator circuit **206** is a measure of how much the OLED **222** has aged.

FIG. **4**D is a timing diagram showing the signals applied to the extraction circuit **200** to extract the turn-on voltage from the OLED **222** via a direct read. FIG. **4**D shows the three phases of the readout process, a pre-charge phase **486**, an integrate phase **487** and a read phase **488**. FIG. **4**D includes a signal **489***n* or **489***p* for the select input **230** in FIG. **2**, a signal **490** (ϕ_1) to the switch **260**, a signal **491** (ϕ_2) for the switch **262**, a signal **492** (ϕ_3) for the switch **264**, a signal **493** (ϕ_4) for the switch **254**, a programming voltage signal **494***n* or **494***p* for the programming data input **232** in FIG. **2**, a voltage **495** of the node **244** in FIG. **2** and an output voltage signal **496** for the output **256** of the amplifier **250** in FIG. **2**.

The process starts by activating the select signal corresponding to the desired row of pixels in array **102**. As illustrated in FIG. **4**D, the select signal **489***n* is active high for an n-type select transistor and active low for a p-type select transistor. A high select signal **489***n* is applied to the select input **230** in the case of an n-type drive transistor. A low signal **489***p* is applied to the select input **230** in the case of a p-type drive transistor for the drive transistor **220**.

The select signal **489***n* or **489***p* will be kept active during the pre-charge and integrate cycles **486** and **487**. The ϕ_1 and ϕ_2 inputs **490** and **491** are inactive in this readout method. During the pre-charge cycle, the switch signals **492** ϕ_3 and **493** ϕ_4 are set high in order to provide a signal path such that the parasitic capacitance **242** of the supply line (C_p) and the voltage at the node **244** are pre-charged to the common-mode voltage (VCM_{OLED}) provided to the non-inverting terminal of the amplifier **250**. A high enough drive voltage signal **494***n* or **494***p* (V_{ON_nTFT} or V_{ON_pTFT}) is applied to the data input **232** (V_{Data}) to operate the drive transistor **220** as an analog switch. Consequently, the supply voltage **212** VD and the node **244** are pre-charged to the common-mode voltage (VCM_{OLED}) to get ready for the next cycle. At the beginning of the integrate phase **487**, the switch input **493** ϕ_4 is turned off in order to allow the charge-pump module **206** to integrate the current of the OLED **222**. The output voltage **496** of the charge-pump module **206** will incline at a constant rate which is a function of the turn-on voltage of the OLED **222** and the voltage **495** set on the node **244**, i.e. VCM_{OLED}. Before the end of the integrate phase **487**, the switch signal **492** ϕ_3 is turned off to isolate the charge-pump module **206** from the pixel circuit **202**. From this instant beyond, the output voltage is constant until the charge-pump module **206** is reset for another reading. When integrated over a certain time period, the output voltage of the integrator is given by:

$$V_{out} = I_{OLED}\frac{T_{int}}{C_{int}}$$

which is a measure of how much the OLED has aged. T_{int} in this equation is the time interval between the falling edge of the switch signal **493** (ϕ_4) to the falling edge of the switch signal **492** (ϕ_3).

Similar extraction processes of a two transistor type driver circuit such as that in FIG. **2** may be utilized to extract non-uniformity and aging parameters such as threshold voltages and mobility of a three transistor type driver circuit as part of the data extraction system **500** as shown in FIG. **5**. The data extraction system **500** includes a drive circuit **502** and a readout circuit **504**. The readout circuit **504** is part of the current supply and readout circuit **120** and gathers data from a column of pixels **104** as shown in FIG. **1** and includes a charge pump circuit **506** and a switch-box circuit **508**. A voltage source **510** provides the supply voltage (VDD) to the drive circuit **502**. The charge-pump and switch-box circuits **506** and **508** are implemented on the top or bottom side of the array **102** such as in the voltage drive **114** and the current supply and readout circuit **120** in FIG. **1**. This is achieved by either direct fabrication on the same substrate as for the array **102** or by bonding a microchip on the substrate or a flex as a hybrid solution.

The drive circuit **502** includes a drive transistor **520**, an organic light emitting device **522**, a drain storage capacitor **524**, a source storage capacitor **526** and a select transistor **528**. A select line input **530** is coupled to the gate of the select transistor **528**. A programming input **532** is coupled through the select transistor **528** to the gate of the drive transistor **220**. The select line input **530** is also coupled to the gate of an output transistor **534**. The output transistor **534** is coupled to the source of the drive transistor **520** and a voltage monitoring output line **536**. The drain of the drive transistor **520** is coupled to the supply voltage source **510** and the source of the drive transistor **520** is coupled to the OLED **522**. The source storage capacitor **526** is coupled between the gate and the source of the drive transistor **520**. The drain storage capacitor **524** is coupled between the gate and the drain of the drive transistor **520**. The OLED **522** has a parasitic capacitance that is modeled as a capacitor **540**. The monitor output voltage line **536** also has a parasitic capacitance that is modeled as a capacitor **542**. The drive transistor **520** in this example is a thin film transistor that is fabricated from amorphous silicon. A voltage node **544** is the point between the source terminal of the drive transistor **520** and the OLED **522**. In this example, the drive transistor **520** is an n-type transistor. The system **500** may be implemented with a p-type drive transistor in place of the drive transistor **520**.

The readout circuit **504** includes the charge-pump circuit **506** and the switch-box circuit **508**. The charge-pump circuit **506** includes an amplifier **550** which has a capacitor **552** (C_{int}) in a negative feedback loop. A switch **554** (S4) is utilized to discharge the capacitor **552** C_{int} during the pre-charge phase. The amplifier **550** has a negative input coupled to the capacitor **552** and the switch **554** and a positive input coupled to a common mode voltage input **558** (VCM). The amplifier **550** has an output **556** that is indicative of various extracted factors of the drive transistor **520** and OLED **522** as will be explained below.

The switch-box circuit **508** includes several switches **560**, **562** and **564** to direct the current to and from the drive circuit **502**. The switch **560** is used during the reset phase to provide the discharge path to ground. The switch **562** provides the supply connection during normal operation of the pixel **104** and also during the integration phase of the readout process. The switch **564** is used to isolate the charge-pump circuit **506** from the supply line voltage source **510**.

In the three transistor drive circuit **502**, the readout is normally performed through the monitor line **536**. The readout can also be taken through the voltage supply line from the supply voltage source **510** similar to the process of timing signals in FIG. **3**A-**3**C. Accurate timing of the input signals (ϕ_1-ϕ_4) to the switches **560**, **562**, **564** and **554**, the select input **530** and the programming voltage input **532** (V_{Data}) is used to control the performance of the readout circuit **500**. Certain voltage levels are applied to the programming data input **532** (V_{Data}) and the common mode voltage input **558** (VCM) during each phase of readout process.

The three transistor drive circuit **502** may be programmed differentially through the programming voltage input **532** and the monitoring output **536**. Accordingly, the reset and pre-charge phases may be merged together to form a reset/pre-charge phase and which is followed by an integrate phase and a read phase.

FIG. **6**A is a timing diagram of the signals involving the extraction of the threshold voltage and mobility of the drive transistor **520** in FIG. **5**. The timing diagram includes voltage signals **602**-**618** for the select input **530**, the switches **560**, **562**, **564** and **554**, the programming voltage input **532**, the voltage at the gate of the drive transistor **520**, the voltage at the node **544** and the output voltage **556** in FIG. **5**. The readout process in FIG. **6**A has a pre-charge phase **620**, an integrate phase **622** and a read phase **624**. The readout process initiates by simultaneous precharging of the drain capacitor **524**, the source capacitor **526**, and the parasitic capacitors **540** and **542**. For this purpose, the select line voltage **602** and the signals **608** and **610** (ϕ_3, ϕ_4) to the switches **564** and **554** are activated as shown in FIG. **6**A. The signals **604** and **606** (ϕ_1, ϕ_2) to the switches **560** and **562** remain low throughout the readout cycle.

The voltage level of the common mode input **558** (VCM) determines the voltage on the output monitor line **536** and hence the voltage at the node **544**. The voltage to the common mode input **558** (VCM_{TFT}) should be low enough such that the OLED **522** does not turn on. In the pre-charge phase **620**, the voltage signal **612** to the programming voltage input **532** (V_{Data}) is high enough (V_{RST_TFT}) to turn the drive transistor **520** on, and also low enough such that the OLED **522** always stays off.

At the beginning of the integrate phase **622**, the voltage **602** to the select input **530** is deactivated to allow a charge to be stored on the capacitor **540** (C_{OLED}). The voltage at the node **544** will start to rise and the gate voltage of the drive transistor **520** will follow that with a ratio of the capacitance value of the source capacitor **526** over the capacitance of the source capacitor **526** and the drain capacitor **524** [$C_{S1}/(C_{S1}+C_{S2})$]. The charging will complete once the difference between the gate voltage of the drive transistor **520** and the voltage at node **544** is equal to the threshold voltage of the drive transistor **520**. Before the end of the integration phase **622**, the signal **610** (ϕ_4) to the switch **554** is turned off to prepare the charge-pump amplifier **550** for the read phase **624**.

For the read phase **624**, the signal **602** to the select input **530** is activated once more. The voltage signal **612** on the programming input **532** (V_{RA_TFT}) is low enough to keep the drive transistor **520** off. The charge stored on the capacitor **240** (C_{OLED}) is now transferred to the capacitor **254** (C_{INT}) and creates an output voltage **618** proportional to the threshold voltage of the drive transistor **520**:

$$V_{out} = -\frac{C_{oled}}{C_{int}}(V_G - V_{th})$$

Before the end of the read phase **624**, the signal **608** (ϕ_3) to the switch **564** turns off to isolate the charge-pump circuit **506** from the drive circuit **502**.

FIG. **6**B is a timing diagram for the input signals for extraction of the turn-on voltage of the OLED **522** in FIG. **5**. FIG. **6**B includes voltage signals **632**-**650** for the select input **530**, the switches **560**, **562**, **564** and **554**, the programming voltage input **532**, the voltage at the gate of the drive transistor **520**, the voltage at the node **544**, the common mode voltage input **558**, and the output voltage **556** in FIG. **5**. The readout process in FIG. **6**B has a pre-charge phase **652**, an integrate phase **654** and a read phase **656**. Similar to the readout for the drive transistor **220** in FIG. **6**A, the readout process starts with simultaneous precharging of the drain capacitor **524**, the source capacitor **526**, and the parasitic capacitors **540** and **542** in the pre-charge phase **652**. For this purpose, the signal **632** to the select input **530** and the signals **638** and **640** (ϕ_3, ϕ_4) to the switches **564** and **554** are activated as shown in FIG. **6**B. The signals **634** and **636** (ϕ_1, ϕ_2) remain low throughout the readout cycle. The input voltage **648** (VCM_{Pre}) to the common mode voltage input **258** should be high enough such that the OLED **522** is turned on. The voltage **642** (V_{Pre_OLED}) to the programming input **532** (V_{Data}) is low enough to keep the drive transistor **520** off.

At the beginning of the integrate phase **654**, the signal **632** to the select input **530** is deactivated to allow a charge to be stored on the capacitor **540** (C_{OLED}). The voltage at the node **544** will start to fall and the gate voltage of the drive transistor **520** will follow with a ratio of the capacitance value of the source capacitor **526** over the capacitance of the source capacitor **526** and the drain capacitor **524** [$C_{S1}/(C_{S1}+C_{S2})$]. The discharging will complete once the voltage at node **544** reaches the ON voltage (V_{OLED}) of the OLED **522**. Before the end of the integration phase **654**, the signal **640** (ϕ_4) to the switch **554** is turned off to prepare the charge-pump circuit **506** for the read phase **656**.

For the read phase **656**, the signal **632** to the select input **530** is activated once more. The voltage **642** on the (V_{RD_OLED}) programming input **532** should be low enough to keep the drive transistor **520** off. The charge stored on the capacitor **540** (C_{OLED}) is then transferred to the capacitor **552** (C_{INT}) creating an output voltage **650** at the amplifier output **556** proportional to the ON voltage of the OLED **522**.

$$V_{out} = -\frac{C_{oled}}{C_{int}} \cdot V_{ON,oled}$$

The signal **638** (ϕ_3) turns off before the end of the read phase **656** to isolate the charge-pump circuit **508** from the drive circuit **502**.

As shown, the monitor output transistor **534** provides a direct path for linear integration of the current for the drive transistor **520** or the OLED **522**. The readout may be carried out in a pre-charge and integrate cycle. However, FIG. **6**C shows timing diagrams for the input signals for an additional final read phase which may be eliminated if the output of charge-pump circuit **508** is sampled at the of the integrate phase. FIG. **6**C includes voltage signals **660**-**674** for the select input **530**, the switches **560**, **562**, **564** and **554**, the programming voltage input **532**, the voltage at the node **544**,

and the output voltage **556** in FIG. **5**. The readout process in FIG. **6**C therefore has a pre-charge phase **676**, an integrate phase **678** and an optional read phase **680**.

The direct integration readout process of the n-type drive transistor **520** in FIG. **5** as shown in FIG. **6**C is initiated by simultaneous precharging of the drain capacitor **524**, the source capacitor **526**, and the parasitic capacitors **540** and **542**. For this purpose, the signal **660** to the select input **530** and the signals **666** and **668** (ϕ_3, ϕ_4) to the switches **564** and **554** are activated as shown in FIG. **6**C. The signals **662** and **664** (ϕ_1, ϕ_2) to the switches **560** and **562** remain low throughout the readout cycle. The voltage level of the common mode voltage input **558** (VCM) determines the voltage on the monitor output line **536** and hence the voltage at the node **544**. The voltage signal (VCM_{TFT}) of the common mode voltage input **558** is low enough such that the OLED **522** does not turn on. The signal **670** (V_{ON_TFT}) to the programming input **532** (V_{Data}) is high enough to turn the drive transistor **520** on.

At the beginning of the integrate phase **678**, the signal **668** (ϕ_4) to the switch **554** is turned off in order to allow the charge-pump amplifier **550** to integrate the current from the drive transistor **520**. The output voltage **674** of the charge-pump amplifier **550** declines at a constant rate which is a function of the threshold voltage, mobility and the gate-to-source voltage of the drive transistor **520**. Before the end of the integrate phase, the signal **666** (ϕ_3) to the switch **564** is turned off to isolate the charge-pump circuit **508** from the drive circuit **502**. Accordingly, the output voltage is given by:

$$V_{out} = -I_{TFT} \cdot \frac{T_{int}}{C_{int}}$$

where I_{TFT} is the drain current of drive transistor **520** which is a function of the mobility and (V_{Data}–V_{CM}–V_{th}). T_{int} is the length of the integration time. The output voltage **674**, which is a function of the mobility and threshold voltage of the drive transistor **520**, may be sampled any time during the read phase **680**.

FIG. **6**D shows a timing diagram of input signals for the direct reading of the on (threshold) voltage of the OLED **522** in FIG. **5**. FIG. **6**D includes voltage signals **682**-**696** for the select input **530**, the switches **560**, **562**, **564** and **554**, the programming voltage input **532**, the voltage at the node **544**, and the output voltage **556** in FIG. **5**. The readout process in FIG. **6**C has a pre-charge phase **697**, an integrate phase **698** and an optional read phase **699**.

The readout process in FIG. **6**D is initiated by simultaneous precharging of the drain capacitor **524**, the source capacitor **526**, and the parasitic capacitors **540** and **542**. For this purpose, the signal **682** to the select input **530** and the signals **688** and **690** (ϕ_3, ϕ_4) to the switches **564** and **554** are activated as shown in FIG. **6**D. The signals **684** and **686** (ϕ_1, ϕ_2) remain low throughout the readout cycle. The voltage level of the common mode voltage input **558** (VCM) determines the voltage on the monitor output line **536** and hence the voltage at the node **544**. The voltage signal (VCM_{OLED}) of the common mode voltage input **558** is high enough such to turn the OLED **522** on. The signal **692** (V_{OFF_TFT}) of the programming input **532** (V_{Data}) is low enough to keep the drive transistor **520** off.

At the beginning of the integrate phase **698**, the signal **690** (ϕ_4) to the switch **552** is turned off in order to allow the charge-pump amplifier **550** to integrate the current from the OLED **522**. The output voltage **696** of the charge-pump amplifier **550** will incline at a constant rate which is a function of the threshold voltage and the voltage across the OLED **522**.

Before the end of the integrate phase **698**, the signal **668** (ϕ_3) to the switch **564** is turned off to isolate the charge-pump circuit **508** from the drive circuit **502**. Accordingly, the output voltage is given by:

$$V_{out} = I_{OLED} \cdot \frac{T_{int}}{C_{int}}$$

where I_{OLED} is the OLED current which is a function of (V_{CM}–V_{th}), and T_{int} is the length of the integration time. The output voltage, which is a function of the threshold voltage of the OLED **522**, may be sampled any time during the read phase **699**.

The controller **112** in FIG. **1** may be conveniently implemented using one or more general purpose computer systems, microprocessors, digital signal processors, microcontrollers, application specific integrated circuits (ASIC), programmable logic devices (PLD), field programmable logic devices (FPLD), field programmable gate arrays (FPGA) and the like, programmed according to the teachings as described and illustrated herein, as will be appreciated by those skilled in the computer, software and networking arts.

In addition, two or more computing systems or devices may be substituted for any one of the controllers described herein. Accordingly, principles and advantages of distributed processing, such as redundancy, replication, and the like, also can be implemented, as desired, to increase the robustness and performance of controllers described herein. The controllers may also be implemented on a computer system or systems that extend across any network environment using any suitable interface mechanisms and communications technologies including, for example telecommunications in any suitable form (e.g., voice, modem, and the like), Public Switched Telephone Network (PSTNs), Packet Data Networks (PDNs), the Internet, intranets, a combination thereof, and the like.

The operation of the example data extraction process, will now be described with reference to the flow diagram shown in FIG. **7**. The flow diagram in FIG. **7** is representative of example machine readable instructions for determining the threshold voltages and mobility of a simple driver circuit that allows maximum aperture for a pixel **104** in FIG. **1**. In this example, the machine readable instructions comprise an algorithm for execution by: (a) a processor, (b) a controller, and/or (c) one or more other suitable processing device(s). The algorithm may be embodied in software stored on tangible media such as, for example, a flash memory, a CD-ROM, a floppy disk, a hard drive, a digital video (versatile) disk (DVD), or other memory devices, but persons of ordinary skill in the art will readily appreciate that the entire algorithm and/or parts thereof could alternatively be executed by a device other than a processor and/or embodied in firmware or dedicated hardware in a well known manner (e.g., it may be implemented by an application specific integrated circuit (ASIC), a programmable logic device (PLD), a field programmable logic device (FPLD), a field programmable gate array (FPGA), discrete logic, etc.). For example, any or all of the components of the extraction sequence could be implemented by software, hardware, and/or firmware. Also, some or all of the machine

readable instructions represented by the flowchart of FIG. **7** may be implemented manually. Further, although the example algorithm is described with reference to the flowchart illustrated in FIG. **7**, persons of ordinary skill in the art will readily appreciate that many other methods of implementing the example machine readable instructions may alternatively be used. For example, the order of execution of the blocks may be changed, and/or some of the blocks described may be changed, eliminated, or combined.

A pixel **104** under study is selected by turning the corresponding select and programming lines on (**700**). Once the pixel **104** is selected, the readout is performed in four phases. The readout process begins by first discharging the parasitic capacitance across the OLED (C_{oled}) in the reset phase (**702**). Next, the drive transistor is turned on for a certain amount of time which allows some charge to be accumulated on the capacitance across the OLED C_{oled} (**704**). In the integrate phase, the select transistor is turned off to isolate the charge on the capacitance across the OLED C_{oled} and then the line parasitic capacitance (C_P) is precharged to a known voltage level (**706**). Finally, the drive transistor is turned on again to allow the charge on the capacitance across the OLED C_{oled} to be transferred to the charge-pump amplifier output in a read phase (**708**). The amplifier's output represent a quantity which is a function of mobility and threshold voltage. The readout process is completed by deselecting the pixel to prevent interference while other pixels are being calibrated (**710**).

FIG. **8** is a flow diagram of different extraction cycles and parameter applications for pixel circuits such as the two transistor circuit in FIG. **2** and the three transistor circuit in FIG. **5**. One process is an in-pixel integration that involves charge transfer (**800**). A charge relevant to the parameter of interest is accumulated in the internal capacitance of the pixel (**802**). The charge is then transferred to the external read-out circuit such as the charge-pump or integrator to establish a proportional voltage (**804**). Another process is an off-pixel integration or direct integration (**810**). The device current is directly integrated by the external read-out circuit such as the charge-pump or integrator circuit (**812**).

In both processes, the generated voltage is post-processed to resolve the parameter of interest such as threshold voltage or mobility of the drive transistor or the turn-on voltage of the OLED (**820**). The extracted parameters may be then used for various applications (**822**). Examples of using the parameters include modifying the programming data according to the extracted parameters to compensate for pixel variations (**824**). Another example is to pre-age the panel of pixels (**826**). Another example is to evaluate the process yield of the panel of pixels after fabrication (**828**).

FIG. **9** is a block diagram and chart of the components of a data extraction system that includes a pixel circuit **900**, a switch box **902** and a readout circuit **904** that may be a charge pump/integrator. The building components (**910**) of the pixel circuit **900** include an emission device such as an OLED, a drive device such as a drive transistor, a storage device such as a capacitor and access switches such as a select switch. The building components **912** of the switch box **902** include a set of electronic switches that may be controlled by external control signals. The building components **914** of the readout circuit **904** include an amplifier, a capacitor and a reset switch.

The parameters of interest may be stored as represented by the box **920**. The parameters of interest in this example may include the threshold voltage of the drive transistor, the mobility of the drive transistor and the turn-on voltage of the OLED. The functions of the switch box **902** are represented by the box **922**. The functions include steering current in and out of the pixel circuit **900**, providing a discharge path between the pixel circuit **900** and the charge-pump of the readout circuit **904** and isolating the charge-pump of the readout circuit **904** from the pixel circuit **900**. The functions of the readout circuit **904** are represented by the box **924**. One function includes transferring a charge from the internal capacitance of the pixel circuit **900** to the capacitor of the readout circuit **904** to generate a voltage proportional to that charge in the case of in-pixel integration as in steps **800-804** in FIG. **8**. Another function includes integrating the current of the drive transistor or the OLED of the pixel circuit **900** over a certain time in order to generate a voltage proportional to the current as in steps **810-814** of FIG. **8**.

While particular embodiments and applications of the present invention have been illustrated and described, it is to be understood that the invention is not limited to the precise construction and compositions disclosed herein and that various modifications, changes, and variations can be apparent from the foregoing descriptions without departing from the spirit and scope of the invention as defined in the appended claims.

What is claimed is:

1. A data extraction system for an organic light emitting device (OLED) based display, the system comprising:

a pixel circuit including an OLED, a drive transistor to provide a programmable drive current to the OLED, a programming input to receive a programming signal, and a storage device to store the programming signal;

a readout circuit including an input and including an output for providing an output voltage value;

a switch module including an input coupled to an output of the pixel circuit and including an output coupled to the input of the readout circuit; and

a controller coupled to the pixel circuit, the readout circuit, and the switch module, the controller operable to control input signals to the pixel circuit, readout circuit, and switch module in a predetermined sequence including a program voltage provided to the programming input to control the pixel circuit to provide a signal output to the input of the readout circuit via the switch module to produce the output voltage value such that it is a function of at least one parameter of the pixel circuit,

wherein the controller is operable to control the program voltage provided to the programming input and to control the input signals, to pre-charge an internal capacitance of the pixel circuit generating a stored charge in the internal capacitance, and to transfer at least a portion of the stored charge to the readout circuit via the switch module, the transferred charge a function of the at least one parameter of the pixel circuit and the output voltage value a function of the transferred charge.

2. A data extraction system for an organic light emitting device (OLED) based display, the system comprising:

a pixel circuit including an OLED, a drive transistor to provide a programmable drive current to the OLED, a programming input to receive a programming signal, and a storage device to store the programming signal;

a readout circuit including an input and including an output for providing an output voltage value;

a switch module including an input coupled to an output of the pixel circuit and including an output coupled to the input of the readout circuit; and

a controller coupled to the pixel circuit, the readout circuit, and the switch module, the controller operable to control input signals to the pixel circuit, readout

circuit, and switch module in a predetermined sequence including a program voltage provided to the programming input to control the pixel circuit to provide a signal output to the input of the readout circuit via the switch module to produce the output voltage value such that it is a function of at least one parameter of the pixel circuit,

wherein the controller is operable to control the program voltage provided to the programming input and to control the input signals, to provide a current from the pixel circuit to the readout circuit via the switch module to produce the output voltage value by integration over a certain period of time, the current a function of the at least one parameter of the pixel circuit, and the output voltage value a function of a capacitance of the readout circuit and the integration time.

3. The system of claim **1**, wherein the program voltage provided to the programming input comprises a programming sequence to produce the output voltage value such that it is a function of the at least one parameter of the pixel circuit.

4. The system of claim **1**, wherein the controller is operable to control the program voltage provided to the programming input and to control the input signals, to allow the stored charge of the internal capacitance to discharge through the switch module to the readout circuit until the gate-to-source drive-voltage of the drive transistor is equal to the threshold voltage of the drive transistor, and wherein the at least one parameter comprises the threshold voltage of the drive transistor, the internal capacitance of the pixel is pre-charged to a level that does not turn the OLED on, and the output voltage value is a function of the threshold voltage, a feedback capacitance of the readout circuit, the OLED capacitance, and the program voltage.

5. The system of claim **1**, wherein the controller is operable to control the program voltage provided to the programming input and to control the input signals, to allow the stored charge of the internal capacitance to partially discharge through the switch module to the readout circuit over an integration time shorter than a substantially complete discharge time for the stored charge, and wherein the at least one parameter comprises the mobility of the drive transistor, the internal capacitance of the pixel is pre-charged to a level that does not turn the OLED on, and the output voltage value is a function of the mobility of the drive transistor, integration time, a feedback capacitance of the readout circuit, and the program voltage.

6. The system of claim **1**, wherein the internal capacitance is the OLED capacitance, and wherein the controller is operable to control the program voltage provided to the programming input and to control the input signals, to discharge the charge on the OLED capacitance through the OLED until it reaches the turn-on voltage of the OLED and transfer the remaining charge on the OLED capacitance through the switch module to the readout circuit, and wherein the at least one parameter comprises the turn-on voltage of the OLED, the OLED capacitance is pre-charged to a level higher than the turn-on voltage of the OLED, and the output voltage value is a function of the turn-on voltage of the OLED, a capacitance in the readout circuit, and the OLED capacitance.

7. The system of claim **2**, wherein the controller is operable to control the program voltage provided to the programming input and to control the input signals, to set the program voltage to a proper level to turn the drive transistor on and steer the current of the drive transistor through the switch module into the readout circuit to be directly integrated for a certain amount of time, and wherein the at least one parameter comprises the threshold voltage and mobility of the drive transistor and the output voltage value is a function of the threshold voltage and mobility and the program voltage.

8. The system of claim **2**, wherein the controller is operable to control the program voltage provided to the programming input and to control the input signals, to set the program voltage to a proper level to operate the drive transistor as a switch and steer the current of the OLED through the switch module into the readout circuit to be directly integrated for a certain amount of time, and wherein the at least one parameter comprises the turn-on voltage of the OLED and the output voltage value is a function of the turn-on voltage of the OLED.

9. A method of extracting data from a pixel circuit of an organic light emitting device (OLED) based display, the pixel circuit including an OLED, a drive transistor to provide a programmable drive current to the OLED, a programming input to receive a programming signal, and a storage device to store the programming signal, the method comprising:

controlling input signals to the pixel circuit, a readout circuit, and a switch module, an output of the pixel circuit coupled to an input of the switch module, an output of the switch module coupled to an input of the readout circuit; and

providing a program voltage to the programming input to control the pixel circuit to provide a signal output to the input of the readout circuit via the switch module to produce an output voltage value from an output of the readout circuit,

the input signals including the program voltage and comprising a predetermined sequence to produce the output voltage value such that it is a function of at least one parameter of the pixel circuit,

wherein the program voltage is provided to the programming input and the input signals are controlled to pre-charge an internal capacitance of the pixel circuit generating a stored charge in the internal capacitance, and to transfer at least a portion of the stored charge to the readout circuit via the switch module, the transferred charge a function of the at least one parameter of the pixel circuit and the output voltage value a function of the transferred charge.

10. A method of extracting data from a pixel circuit of an organic light emitting device (OLED) based display, the pixel circuit including an OLED, a drive transistor to provide a programmable drive current to the OLED, a programming input to receive a programming signal, and a storage device to store the programming signal, the method comprising:

controlling input signals to the pixel circuit, a readout circuit, and a switch module, an output of the pixel circuit coupled to an input of the switch module, an output of the switch module coupled to an input of the readout circuit; and

providing a program voltage to the programming input to control the pixel circuit to provide a signal output to the input of the readout circuit via the switch module to produce an output voltage value from an output of the readout circuit,

the input signals including the program voltage and comprising a predetermined sequence to produce the output voltage value such that it is a function of at least one parameter of the pixel circuit,

wherein the program voltage is provided to the programming input and the input signals are controlled to provide a current from the pixel circuit to the readout circuit via the

switch module to produce the output voltage value by integration over a certain period of time, the current a function of the at least one parameter of the pixel circuit, and the output voltage value a function of a capacitance of the readout circuit and the integration time.

11. The method of claim **9**, wherein the program voltage provided to the programming input comprises a programming sequence to produce the output voltage value such that it is a function of the at least one parameter of the pixel circuit.

12. The method of claim **9**, further comprising:

allowing the stored charge of the internal capacitance to discharge through the switch module to the readout circuit until the gate-to-source drive-voltage of the drive transistor is equal to the threshold voltage of the drive transistor,

wherein the at least one parameter comprises the threshold voltage of the drive transistor, the internal capacitance of the pixel is pre-charged to a level that does not turn the OLED on, and the output voltage value is a function of the threshold voltage, a feedback capacitance of the readout circuit, the OLED capacitance, and the program voltage.

13. The method of claim **9**, further comprising:

allowing the stored charge of the internal capacitance to partially discharge through the switch module to the readout circuit over an integration time shorter than a substantially complete discharge time for the stored charge,

wherein the at least one parameter comprises the mobility of the drive transistor, the internal capacitance of the pixel is pre-charged to a level that does not turn the OLED on, and the output voltage value is a function of the mobility of the drive transistor, integration time, a feedback capacitance of the readout circuit, and the program voltage.

14. The method of claim **9**, wherein the internal capacitance is the OLED capacitance, the method further comprising:

discharging the charge on the OLED capacitance through the OLED until it reaches the turn-on voltage of the OLED; and

transferring the remaining charge on the OLED capacitance through the switch module to the readout circuit,

wherein the at least one parameter comprises the turn-on voltage of the OLED, the OLED capacitance is pre-charged to a level higher than the turn-on voltage of the OLED, and the output voltage value is a function of the turn-on voltage of the OLED, a capacitance in the readout circuit, and the OLED capacitance.

15. The method of claim **10**, further comprising:

setting the program voltage to a proper level to turn the drive transistor on; and

steering the current of the drive transistor through the switch module into the readout circuit to be directly integrated for a certain amount of time,

wherein the at least one parameter comprises the threshold voltage and mobility of the drive transistor and the output voltage value is a function of the threshold voltage and mobility and the program voltage.

16. The method of claim **10**, further comprising:

setting the program voltage to a proper level to operate the drive transistor as a switch; and

steering the current of the OLED through the switch module into the readout circuit to be directly integrated for a certain amount of time,

wherein the at least one parameter comprises the turn-on voltage of the OLED and the output voltage value is a function of the turn on voltage of the OLED.

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专利名称(译)	用于提取AMOLED显示器中的阈值和迁移率参数的系统和方法		
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申请号	US16/175906	申请日	2018-10-31
[标]申请(专利权)人(译)	伊格尼斯创新公司		
申请(专利权)人(译)	IGNIS创新INC.		
当前申请(专利权)人(译)	IGNIS创新INC.		
[标]发明人	CHAJI GHOLAMREZA AZIZI YASER		
发明人	CHAJI, GHOLAMREZA AZIZI, YASER		
IPC分类号	G09G3/00 G09G3/3266 G01R19/00 G09G3/3233 H03F3/217 G09G3/3291 G09G3/3258		
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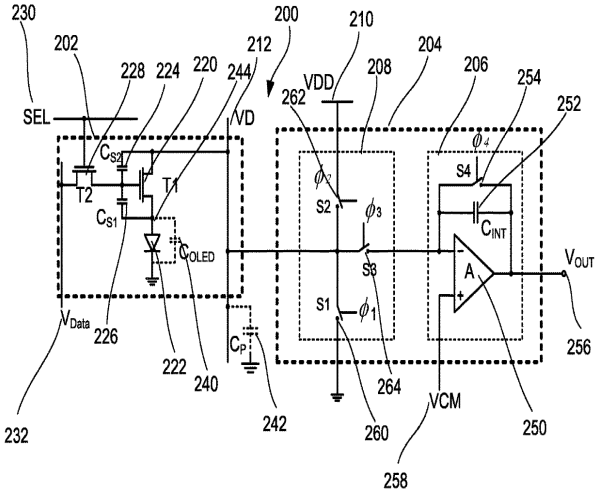
摘要(译)

一种改善AMOLED显示器中晶体管和OLED参数提取的系统，包括：具有有机发光装置的像素电路，向发光装置提供可编程驱动电流的驱动装置，提供编程信号的编程输入， 存储设备，用于存储编程信号。 电荷泵放大器具有电流输入和电压输出。 电荷泵放大器包括负反馈配置的运算放大器。 反馈由连接在运算放大器的输出和反相输入之间的电容器提供。 共模电压源驱动运算放大器的同相输入。 电子开关跨接在电容器两端，以重置电容器。 包括输入的开关模块耦合到像素电路的输出，并且输出耦合到电荷泵放大器的输入。